DSP56305ADM

User's Manual

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This manual is one of a set of three documents. You need the following manuals to have complete product information: Family Manual, User's Manual, and Technical Data.

Order this document by **D56305ADMUM/D**

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SECTION 1

QUICK START GUIDE

1.1 OVERVIEW

The Motorola Application Development System (ADS) is a tool used to design and test complex software applications and hardware products using a specific Motorola DSP chip. The related Application Development Modules (ADMs) contain the DSP chip and related hardware used for bench development and test. Detailed information about the content and use of the ADS is provided in the *ADS User's Manual (DSPADSUM/AD)*. This manual provides specific information about the DSP56305 Application Development Module (DSP56305ADM). This section provides a summary description of the DSP56305ADM, additional requirements, and quick installation information. Detailed information about the DSP56305ADM design and operation is provided in the remaining sections of this manual.

Subsection 1.2 of this document gives a summary description of the equipment required to use the module with the Motorola ADS.

Subsection 1.3 describes installation instructions, including:

- Preparing the module for installation
- Installing the module
- Installing the software
- Testing the installation

Note: Detailed information about the design and operation of the DSP56305ADM is provided in this manual in **Section 2** and **Appendices A** and **B**.

1.2 REQUIRED USER-SUPPLIED EQUIPMENT

The following section gives a brief summary of the equipment required to use the DSP56305 Application Development Module (DSP56305ADM), some of which will be supplied with the module, and some of which must be supplied by the user. For use with the Motorola ADS (and the appropriate interface card), the user must supply one of the following host computer systems:

- PC-compatible computer (486 class or higher) with:
  - MS-DOS version 6.0 or later, Windows 3.1 or later, or Windows 95
  - Minimum 8 Mbytes RAM
  - One open 16-bit ISA expansion slot
  - One bank of free I/O addresses in the range of $100–$102, $200–202, or $300–$303 (no IRQ is required)
  - CD-ROM drive
  - Hard drive with 4 Mbytes of free disk space
  - Mouse
- Sun Microsystems Sun 4 Workstation running Sun Operating System Release 4.1.1 or later (or Solaris Release 2.5 or later), one open SBus expansion slot, a CD-ROM drive, and a mouse
- Hewlett Packard HP7xx Workstation running HPUX Version 9.x (Version 10.x is not supported), one open EISA expansion slot, a CD-ROM drive, and a mouse

1.3 INSTALLATION PROCEDURE

Installation requires the following steps:

1. Preparing the DSP56305ADM board
2. Installing the module
3. Installing the software
4. Testing the installation

1.3.1 Preparing the DSP56305ADM

CAUTION

Because all electronic components are sensitive to the effects of electrostatic discharge (ESD) damage, correct procedures should be used when handling all components in this kit and inside the supporting personal computer. Use the following procedures to minimize the likelihood of damage due to ESD:

- **Always handle all static-sensitive components only in a protected area, preferably a lab with conductive (anti-static) flooring and bench surfaces.**
- **Always use grounded wrist straps when handling sensitive components.**
- **Never remove components from anti-static packaging until required for installation.**
- **Always transport sensitive components in anti-static packaging.**

This procedure describes configuring the DSP56305ADM board for use with its ISA bus interface. The board is factory configured as plug-in card for ISA bus operation. Refer to **Host Port Selection** on page 2-17 for other configurations.

Locate the jumper blocks on the DSP56305ADM board, as shown in **Figure 1-1** and **Figure 1-2** on page 1-8. Verify their settings as shown in **Table 1-1** on page 1-6. See the technical summary in **Section 2** of this manual for additional information about the DSP56305ADM board and its components.

Table 1-1 DSP56305ADM Default Switch / Jumper Options

Group	Default Option	Comment
J1	Removed	512K words optional DRAM disabled
J2	Removed	128K words optional SRAM disabled
J3	Jumpered	128K words SRAM enabled
J4, J5	J4—Removed J5 3–6,4–5	ISA DMA channel 5 selected
J6	4–5	ISA Interrupt channel 10 selected
JP1	1–2	ISA clamp protection is set
JP2	Removed	DSP PLL enabled
JP3 ,JP4, JP5, JP6	Removed	ISA host interface enabled
JP7	Removed	Flash memory disabled
JP8 (located on bottom of board)	1–8	Sets clock source to clock generator
SW3	SW3–2: ON SW3–1, 3, 4: OFF	Bootstraps from Host ISA

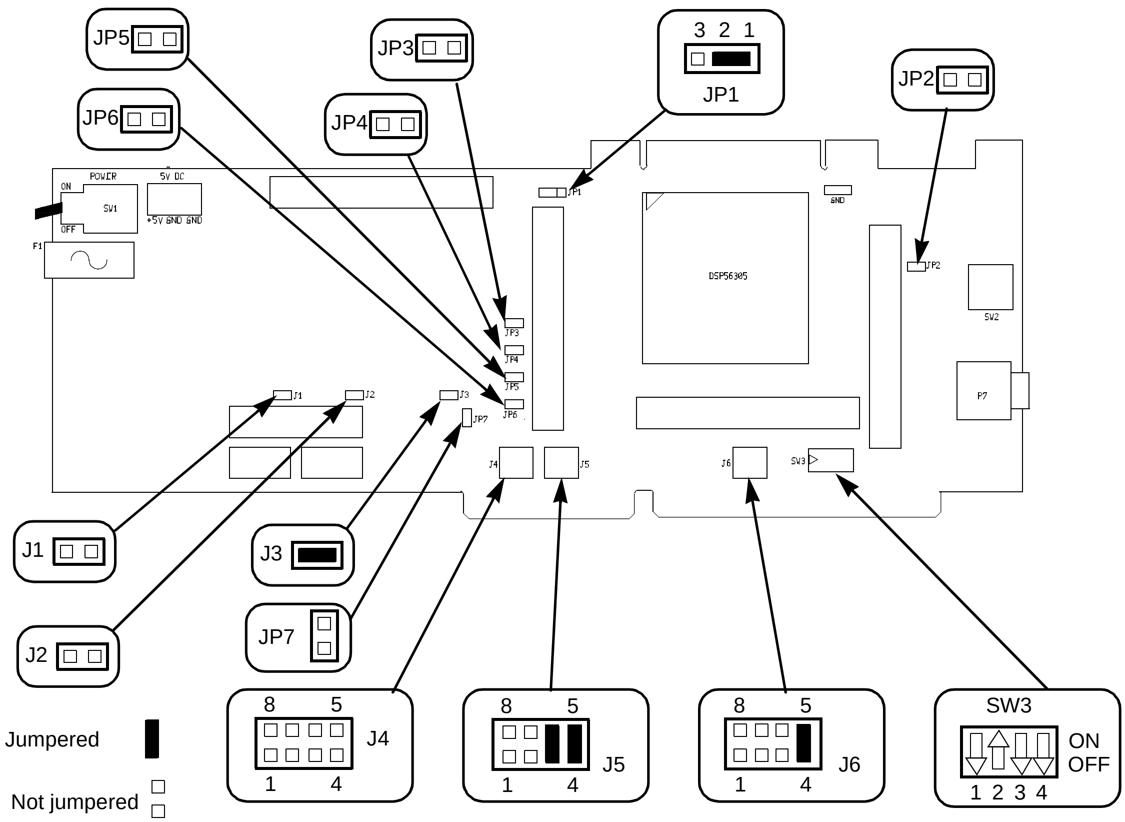


Figure 1-1 Jumper Configuration—Front Side

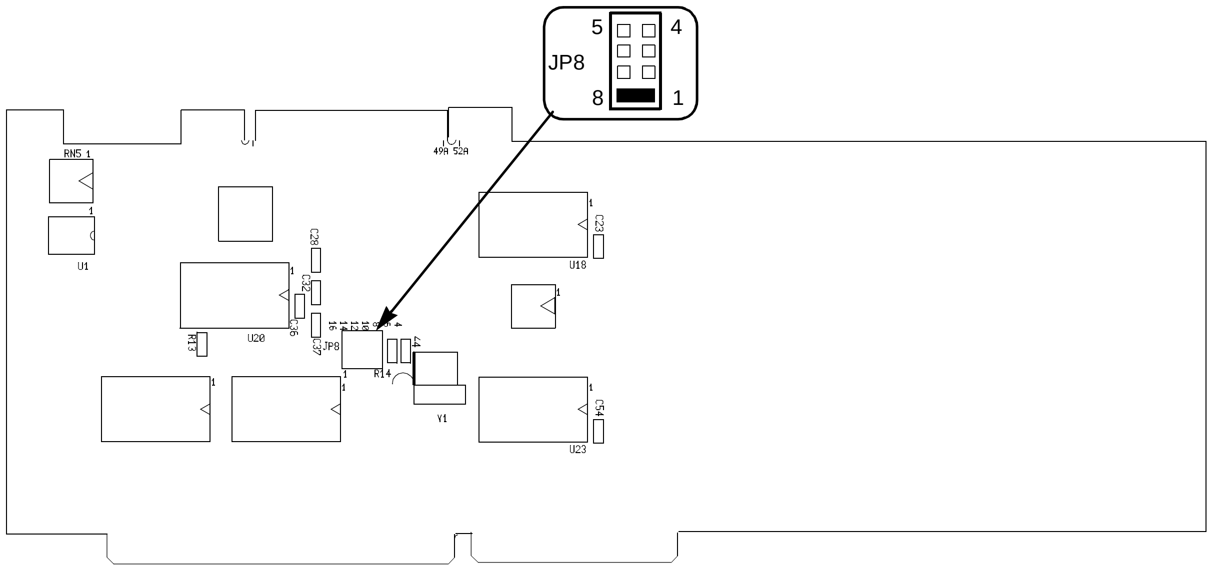


Figure 1-2 Jumper Configuration—Back Side

1.3.2 Installing the DSP56305ADM

Figure 1-3 shows the interconnection diagram for connecting a PC to the DSP56305ADM board. Using the instructions in the ADS User’s Manual, connect the Command Converter to the DSP56305ADM board. Power for the DSP56305ADM is supplied from the Command Converter module.

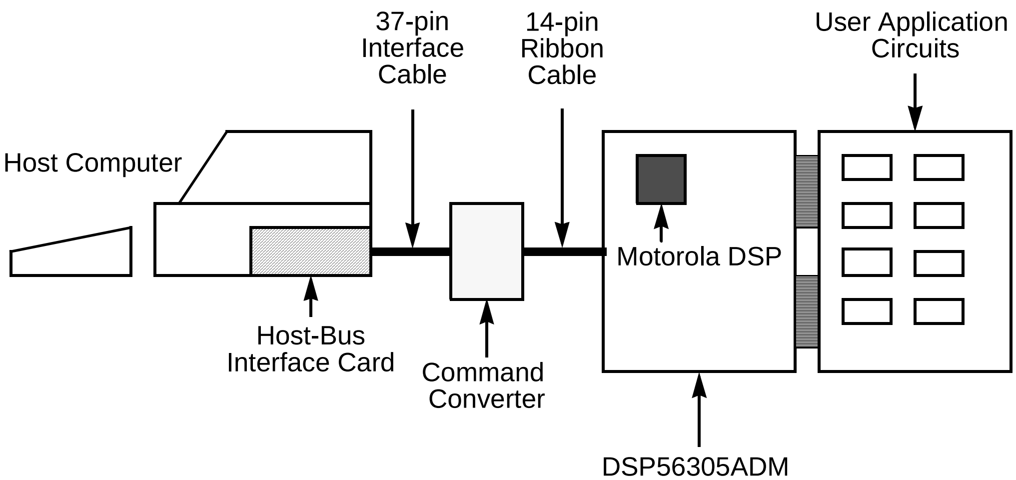


Figure 1-3 Application Development

1.3.3 Installing the Software

Refer to the Motorola *Application Development System User's Manual* for detailed instructions about installation and use of the ADS software.

1.3.4 Testing the DSP56305ADM Installation

Once the DSP56305ADM is installed, it becomes a part of the Application Development System. Refer to the Motorola *Application Development System User's Manual* for detailed information regarding evaluation and testing of an installed ADS system.

SECTION 2

TECHNICAL SUMMARY

2.1 DSP56305ADM BOARD ARCHITECTURE

The DSP56305ADM is a versatile board that can be used as a stand-alone board or as an expansion card in a host computer with ISA or PCI expansion slots, and connected to other cards. The DSP56305 signals, power, and ground connections, are brought out to four 50-pin connectors for attaching additional boards or logic analyzers. In addition, separate connectors are provided for the on-chip peripheral ports—SCI, SSI, and JTAG / OnCE™. A dedicated connector is provided for audio applications. An overview description of the DSP56305 is also provided in the *DSP56305 Product Information (DSP56305P/D)* included with this kit.

2.2 DSP56305ADM FEATURES

The DSP56305ADM provides the following features:

- DSP56305 running at 80 MHz on board (socketed BGA package)
- 128K fast static memory, one wait state access at 80 MHz (3.3V)
- Option to add 128K fast static memory, 1 wait state access at 80 MHz (3.3V)
- Option to add 512K dynamic memory (4–15 wait state access at 80 MHz (3.3V)
- 64K Byte Flash PROM, on-board (3.3V) programmable
- ISA / EISA bus compatible edge-connector (slave only operation)
- PCI bus compatible edge-connector (master and slave operation)
- Stand-alone or computer plug-in card operation
- Integrated expansion and logic-analyzer connectors
- Dedicated SSI ports connectors
- Dedicated SCI port connector
- JTAG / OnCE port connector
- 5V operation, with on-board 3.3 V voltage regulation

Note: Call your local Motorola sale office or distributor for additional information about the Motorola DSP Application Development System (ADS) kit. The ADS kit includes two additional boards: a Host Interface Card, and an external Universal Command Converter. The Host Interface Card plugs into the bus (on an IBM PC-compatible, HP7xx workstation, or Sun / Sun-compatible system) in the computer case. The Host Interface Card is connected via a 37-way ribbon cable to an external Universal Command Converter, which is then connected via a 14-way ribbon cable and the JTAG / OnCE port to the DSP56305ADM. The ADS is compatible only with Motorola software tools.

Figure 2-1 shows the DSP56305ADM architecture. To achieve the best memory performance, no memory decoding is performed outside the DSP56305 chip, and the AA (Address Attribute) lines are used. There is a variety of jumpers options, for various memories configuration, to enable / disable each of the memory types on the DSP56305ADM.

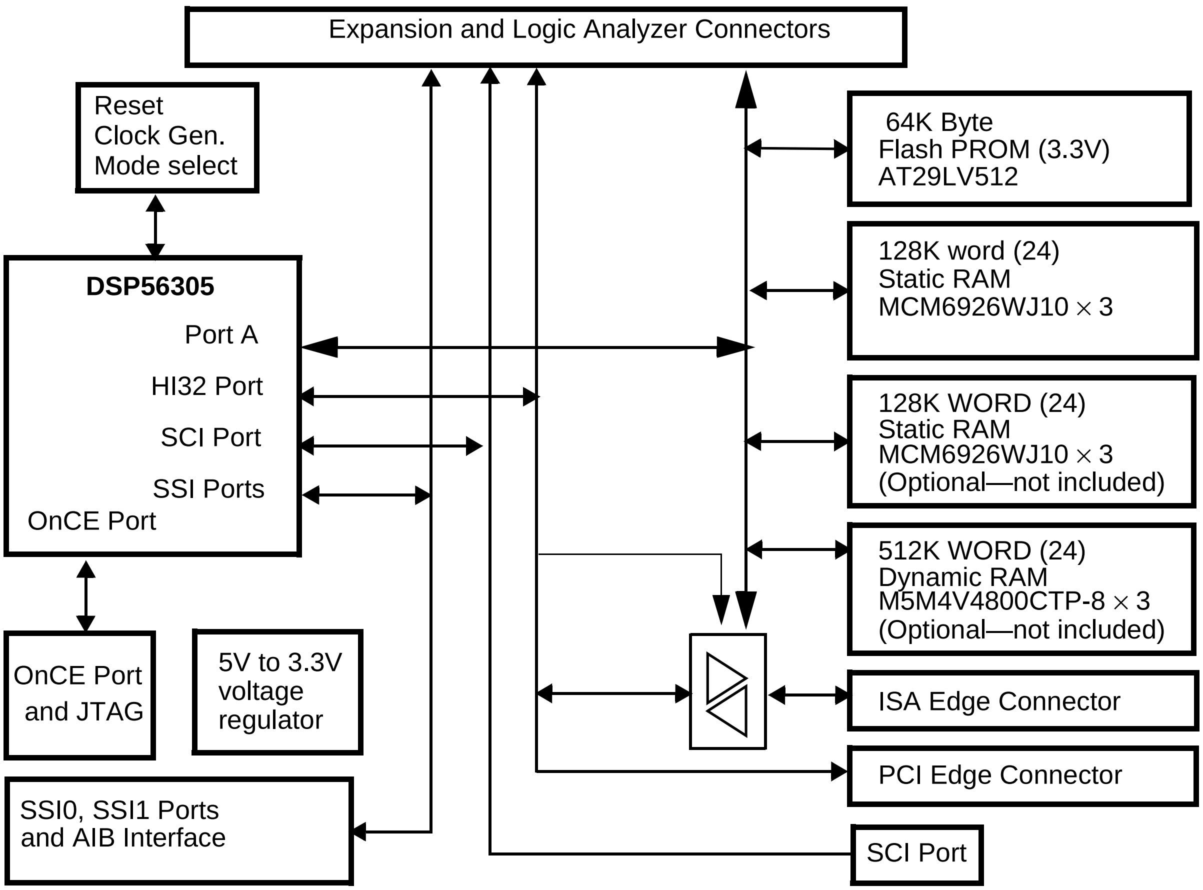


Figure 2-1 DSP56305ADM Block Diagram

2.3 CONFIGURING THE DSP56305 ADM

Figure 1-1 and **Figure 1-2** on page 1-8 show the physical locations of jumpers on the DSP56305ADM. **Table 2-1** describes the default factory configuration for the DSP56305ADM jumper groups.:

Table 2-1 DSP56305 Card Default Switch/Jumper Options

Group	Default Option	Comment
J1	Removed	Disables 512K words optional DRAM memory
J2	Removed	Disables 128K words optional SRAM memory
J3	Mounted	Enables 128K words SRAM memory
J4, J5	J4—no jumpers J5—3–6, 4–5	Sets ISA DMA channel 5 selected
J6	4-5	Sets ISA Interrupt channel 10
JP7	Removed	Disables Flash memory
JP3, JP4, JP5, JP6	Mounted	Enables ISA host interface
JP1	1–2	Sets ISA clamp protection
JP2	Removed	Enables DSP PLL to run
JP8 (located on back)	1–8	Selects clock source to clock generator.
SW3	SW3-2: ON SW3-1,3,4: OFF	Bootstraps from host ISA bus

Figure 2-2 on page 2-6 shows the component placement on the front of the DSP56305ADM. **Figure 2-3** on page 2-7 shows the component placement on the back of the DSP56305ADM.

Note: The board is factory configured as plug-in card for ISA bus operation. Refer to **Host Port Selection** on page 2-17 for other configurations.

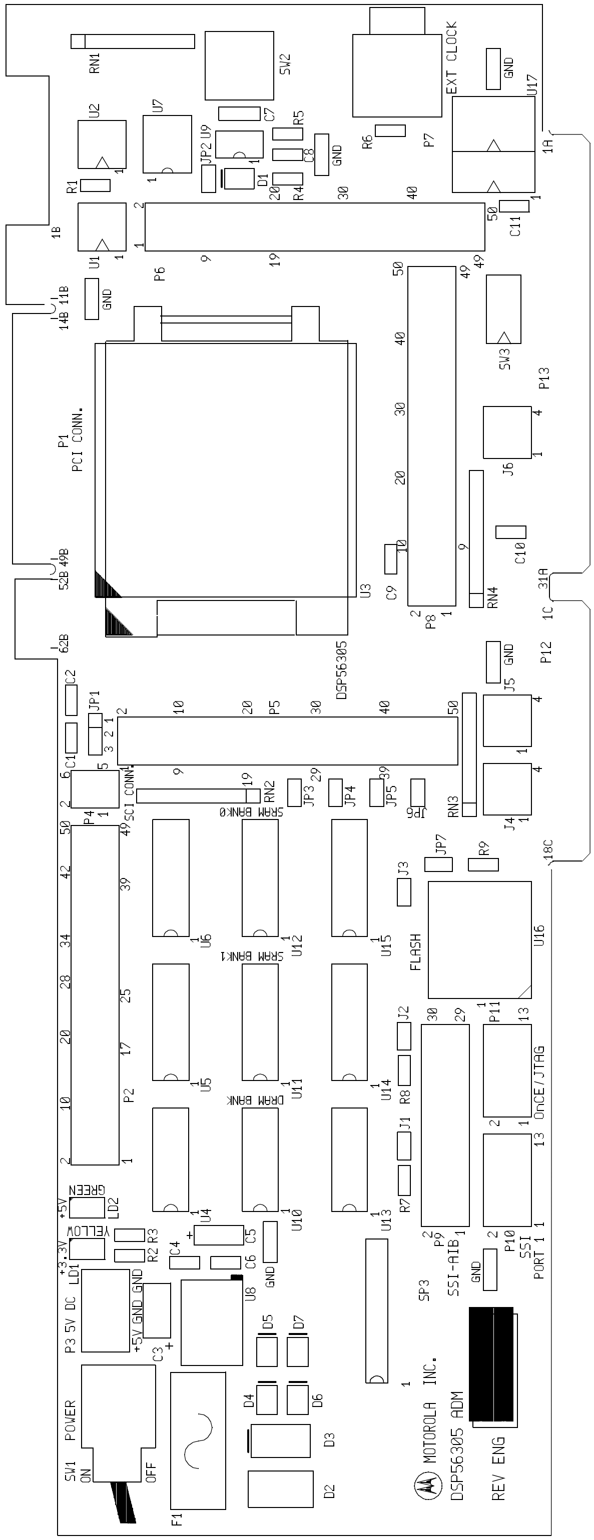


Figure 2-2 DSP56305ADM Top of Board

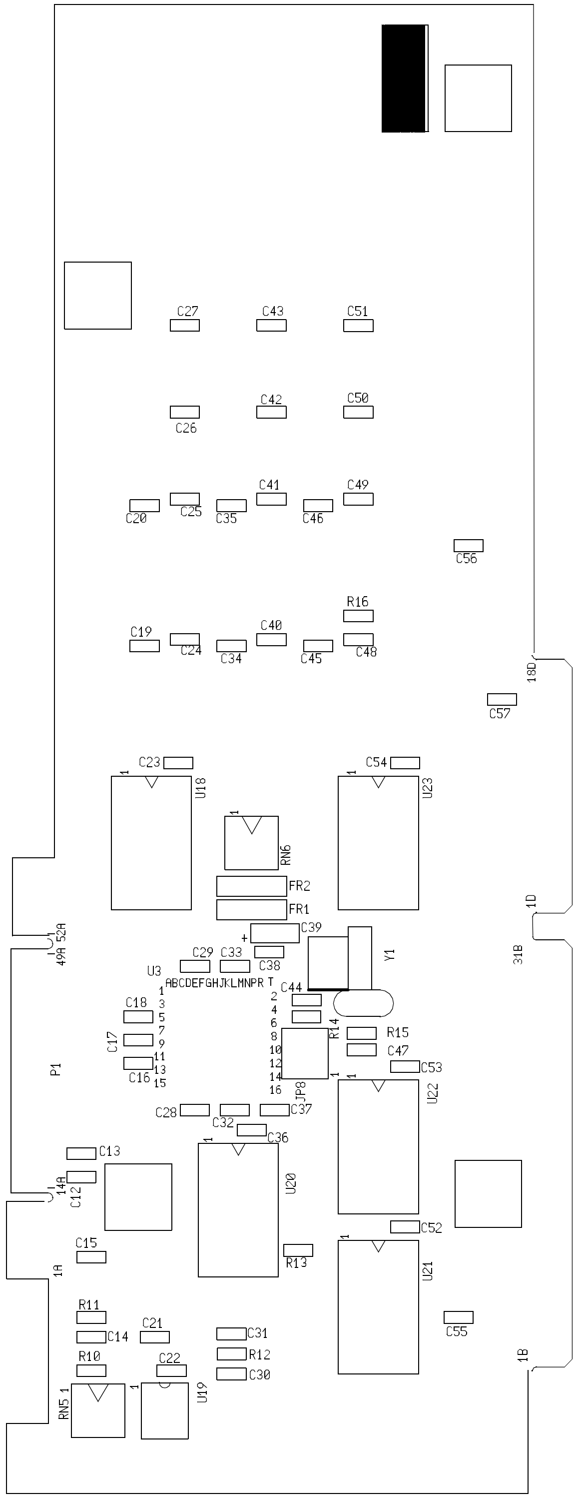


Figure 2-3 DSP56305ADM Bottom of Board

2.4 DSP56305ADM MEMORIES

Table 2-2 DSP56305ADM Memories

Type	Size	Speed	Voltage	AA Line	On Board
SRAM	128K word (24-bit)	10 ns	3.3V	AA0	Constant
SRAM	128K word (24-bit)	10 ns	3.3V	AA3	Optional
DRAM	512K word (24-bit)	80 ns	3.3V	AA2	Optional
Flash	64K byte	200 ns	3.3V	AA1	On Socket
Note:	The first bank of SRAM and the Flash PROM are supplied as standard with the DSP56305ADM. The second SRAM bank and the DRAM are not included. All circuitry and associated components (decoupling capacitors, jumpers, etc.) are provided, with solder pads for mounting the optional SRAM and DRAM chips if desired.				

2.4.1 128K SRAM (With Option for 128K SRAM)

The SRAM on the DSP56305ADM is composed of a single bank of three chips of 128K × 8 SRAM, providing 128K words of 24-bit memory. These chips are MCM6926WJ10, a 3.3 v BiCMOS device with an access time of 10 nsec. The maximum load capacitance of each bank is 3 × 6 pF = 18 pF (address bus) and 8 pF (data bus). The 128K SRAM is accessed by the DSP56305 with one wait state when the DSP operates with an 80 MHz clock. Although devices with 12 ns access time are adequate for 80 MHz operation, a 10 ns device is used to enable operation at 100 MHz. The chip select to the onboard SRAM is generated using the DSP56305 AA0 line. The AA3 line selects the optional 128K block. The 128K SRAM connection is shown in **Figure 2-4**.

SRAM bank 0 comprises a single bank of 3 chips of 128k X 8, 3.3 V devices, providing 128k 24-bit words. The chips used are Motorola MCM6926WJ10. This is a BiCMOS SRAM, 128k x 8, 3.3 V-only device, with an access time of 10 nS. The maximum load capacitance of each bank is 3 x 6 pf = 18 pF (address bus) and 8 pF (data bus). The SRAM is accessed by the DSP56305 with 1 wait-state when the DSP operates at 80 MHz clock. Although devices with 12 nS access time are acceptable for 80 MHz operation, the 10 nS device permits 1 wait state operation with 100 MHz versions of the DSP56305.

The chip-select to SRAM bank 0 is generated using the DSP56305 signal AA0. The power supply to the MCM6926WJ10 is 3.3 V. SOJ packages are used. Schematic detail of SRAM connections is shown in **Figure 2-4**.

Space is provided to mount an additional 128 k words of SRAM as bank 1. Specifications and connection are identical to bank 0, except AA3 provides chip select for bank 1.

Jumper J3 controls SRAM bank 0, and jumper J2 controls optional SRAM bank 1. When the jumper is inserted, the SRAM bank is enabled and the appropriate Address Attribute signal is used as Chip Select. When the jumper is removed, the SRAM bank is disabled and the Address Attribute signal can be used for other purposes.

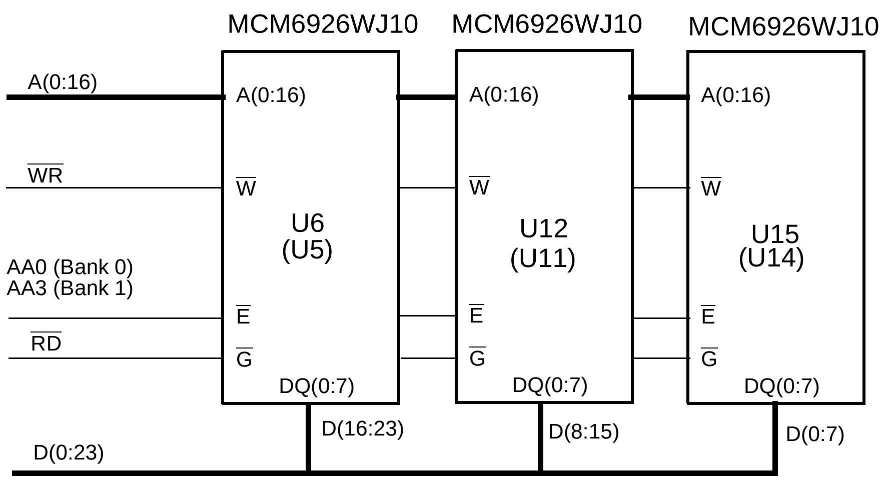


Figure 2-4 128K SRAM Connection

The 128K SRAM is enabled and disabled using jumper J3. J2 is used to enable and disable the optional bank. When the appropriate jumper is installed, its corresponding bank of SRAM is enabled. When the jumper is not installed, the SRAM is disabled, and the AA0 line (or the AA3 line for the optional SRAM bank) can be used for other purposes.

Note: Because of increased capacitance on the data and address lines if the optional SRAM bank is mounted, performance may be degraded.

Table 2-3 SRAM Configuration Jumper Settings

SRAM Configuration	J3	J2
SRAM Bank 0 Enabled	1 [• •] 2	—
SRAM Bank 0 Disabled	1 • • 2	—
SRAM Bank 1 Enabled	—	1 [• •] 2
SRAM Bank 1 Disabled	—	1 • • 2

2.4.2 Optional 512K DRAM

The 512K DRAM on the DSP56305ADM is composed of a single bank of three chips of 512K $\times$ 8, 3.3V,withan access time of 80 nsec. The DRAM chips are M5M4V4800CTP-8. The maximum load capacitance of each bank is 3×5 pf = 15 pF (address bus) and 7 pF (data bus). The 512K DRAM is accessed by the DSP56305 with four wait states when the DSP56305 is operating with an 80 MHz clock. The $\overline{\text{RAS}}$ signal to the 512K DRAM is generated using the DSP56305 AA2 / $\overline{\text{RAS}}$ line.

The 512K DRAM connection is shown in **Figure 2-5**.

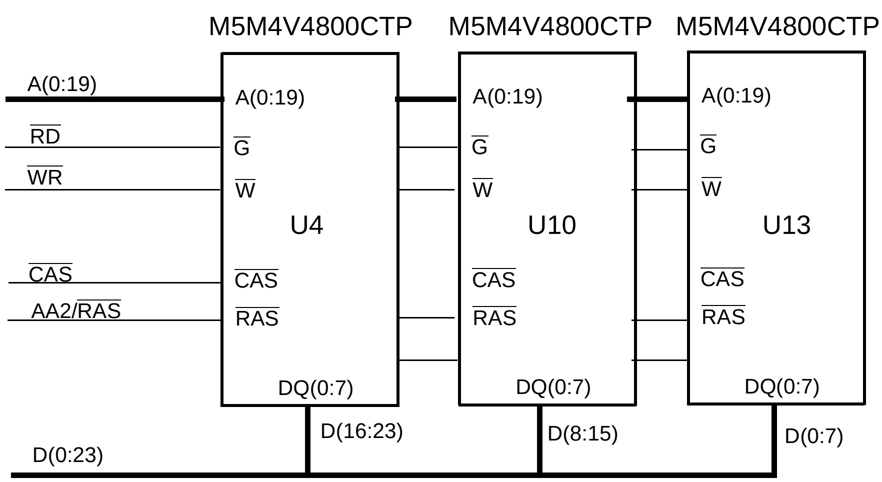


Figure 2-5 512K DRAM Connection

The 512K words DRAM is enabled and disabled using jumper J1. When J1 is installed, the DRAM bank is enabled. When J1 is not installed, the DRAM is disabled, and AA2 line can be used for other purposes. See **Table 2-4** for DRAM jumper configuration.

Table 2-4 DRAM Configuration Jumper Settings

DRAM Configuration	J1
DRAM Bank 0 Enabled	1 ▣ 2
DRAM Bank 0 Disabled	1 • • 2

Note: Because of increased capacitance on the data and address lines if the optional DRAM bank is mounted, performance may be degraded.

2.4.3 Flash PROM

To facilitate stand-alone operation of the DSP56305ADM, a Flash PROM is provided. The FPROM is on-board programmable, making it ideal for updates. Use is done with a byte wide, AT29LV512 3.3V only programmable (eliminating the need for additional supply or a DC-DC converter), 200 nsec access time. The low speed has no performance implications here, since the program is copied by the DSP56305 byte by byte to its internal memory and run from there. The load capacitance of this chip is 6 pF on the address lines and 12 pF (maximum) on the data lines. The flash memory can tolerate as many as 1000 program cycles per sector. Each sector is 128 bytes, for a total of 512 sectors. The AT29LV512 has a low-power write protect against inadvertent write during power transitions. It also features data polling during programming to shorten programming cycles. All actions to the device are controlled via a sequence of commands (except Read state, which the device enters after power-up), written to the device. The Flash PROM is connected to Port A of the DSP56305 as shown in **Figure 2-6**.

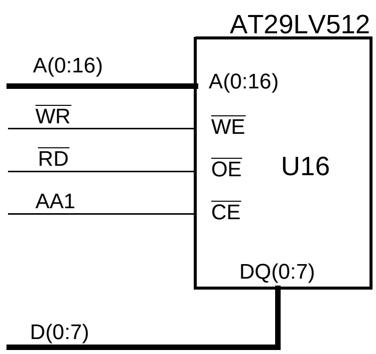


Figure 2-6 Flash PROM Connection

The Flash memory is enabled and disabled using jumper JP7. When JP7 is installed, the Flash memory is enabled. When JP7 is removed, the Flash is disabled, and the AA1 line can be used for other purposes.

Table 2-5 Flash PROM Configuration Jumper Settings

Flash PROM Configuration	JP7
Flash PROM Enabled	1 •-• 2
Flash PROM Disabled	1 • • 2

2.5 DSP56305 OPERATING MODES

All of the operating modes provided on the DSP56305 can be accessed on the DSP56305ADM. For detailed information on the se modes, please see the *DSP56305 User’s Manual (DSP56305UM/D)* and the *DSP56300 Family Manual (DSP56300FM/D).*

During reset, the DSP56305 interrupt signals ($\overline{\mathrm{IRQA}}$–$\overline{\mathrm{IRQD}}$) are also used as the Mode Select signals (MODA–MODD). The DSP56305ADMuses SW3 to select the mode entered on exit from reset. **Table 2-6** lists the available modes.

Multiplexor U13 selects the signals presented on the DSP signals $\overline{\mathrm{IRQA}}$ / MODA–$\overline{\mathrm{IRQD}}$ / MODD. During reset (the $\overline{\mathrm{RESET}}$ signal is asserted), the values selected on SW3 are passed to the DSP56305. The MODx signals are pulled high; closing a switch in SW3 pulls the corresponding MODx signal low. These values are sampled by the DSP56305 on the rising edge of $\overline{\mathrm{RESET}}$, and moved to the Operating Mode Register (OMR). This determines the mode in which the DSP56305 exits reset. During normal operation ($\overline{\mathrm{RESET}}$ deasserted), U13 passes the interrupt signals, $\overline{\mathrm{INTRA}}$–$\overline{\mathrm{INTRD}}$, to the DSP56305 as $\overline{\mathrm{IRQA}}$–$\overline{\mathrm{IRQD}}$.

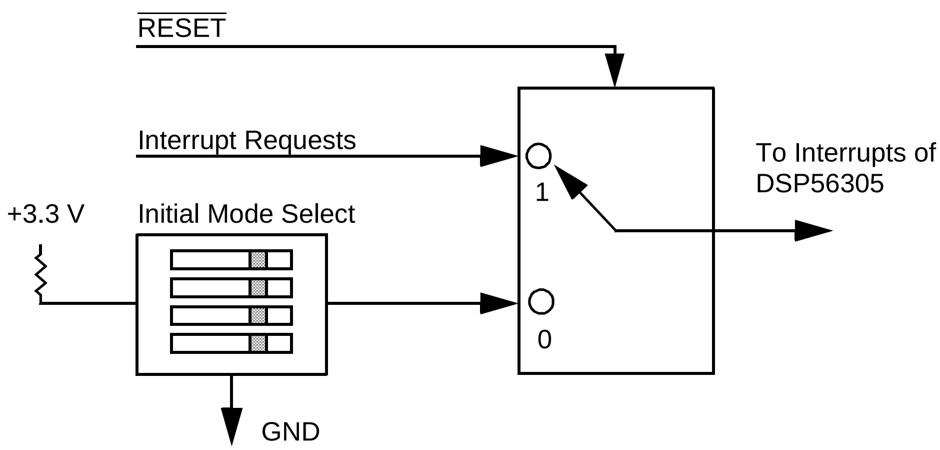


Figure 2-7 DSP Mode Selection Block Diagram

Support is provided to enable DSP56305 to enter to all available modes via MODA / $\overline{\text{IRQA}}$ —MODD / $\overline{\text{IRQD}}$ and $\overline{\text{NMI}}$ / PINIT lines. These lines are sampled by the DSP56305 on the rising edge of the $\overline{\text{RESET}}$ signal. The sampled combination is moved to the Operating Mode Register (OMR). After $\overline{\text{RESET}}$ is deasserted, the mode selection lines are released, driven by pull up resistors and the MOD / $\overline{\text{IRQ}}$ signals are connected to $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ lines.

Table 2-6 Operating Mode Selection.

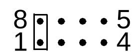
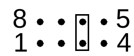
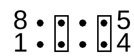
Mode	SW3(1) MODA	SW3(2) MODB	SW3(3) MODC	SW3(4) MODD
0—Expanded mode	ON	ON	ON	ON
1—RTOS Mode	OFF	ON	ON	ON
2—RTOS Mode	ON	OFF	ON	ON
3—RTOS Mode	OFF	OFF	ON	ON
4—(Reserved)	ON	ON	OFF	ON
5—(Reserved)	OFF	ON	OFF	ON
6—(Reserved)	ON	OFF	OFF	ON
7—(Reserved)	OFF	OFF	OFF	ON
8—Expanded mode	ON	ON	ON	OFF
9—Bootstrap from byte-wide memory	OFF	ON	ON	OFF
A—Bootstrap through SCI	ON	OFF	ON	OFF
B—(Reserved)	OFF	OFF	ON	OFF
C—Host Bootstrap PCI Mode (32-bit-wide)	ON	ON	OFF	OFF
D—Host Bootstrap 16-bit-wide UB Mode (ISA)	OFF	ON	OFF	OFF
E—Host Bootstrap 8-bit-wide UB Mode in double-strobe pin configuration	ON	OFF	OFF	OFF
F—Host Bootstrap 8-bit-wide UB Mode in single-strobe pin configuration	OFF	OFF	OFF	OFF

2.6 CLOCK SOURCE

There are three clock sources on the DSP56305ADS:

- Low cost on-board clock generator
- External BNC connector
- Crystal oscillator

Table 2-7 Clock Source Selection Jumper Settings

Clock Source	JP8
Clock Generator	
BNC Connector	
Crystal Oscillator	

The DSP56305ADM is configured for the on-board clock generator, with a DIP14 package, 33.0 MHz, 3.3 V clock generator, and a jumper linking JP8 pins 1–8.

It is recommended that when the on-board clock generator is used, or when an external clock is provided through the BNC connector, the XTLD and COD bits in the PLL Control Register (PCTL) should be set. This helps avoid unnecessary on-board RFI.

2.6.1 On-Board Clock Generator

The clock generator (U17) is mounted in a socket, allowing frequency selection by replacing the clock generator. The user may replace the clock generator with a generator of a different frequency . The PCB layout is designed such that it will accept both 14-pin and 8-pin DIP packages for the clock generator socket.

The DSP56305ADM supports both 8-pin and 14-pin, 3.3 V clock generator modules. Locate the clock generator in the socket as shown in**Figure 2-8**.

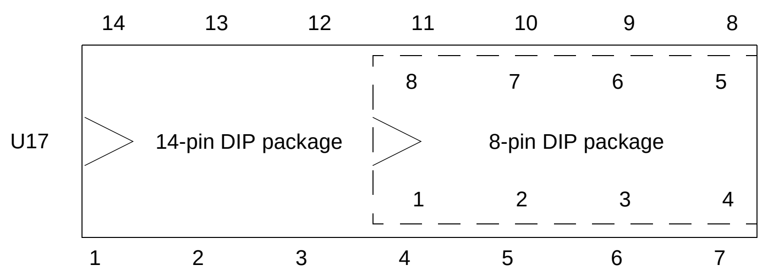


Figure 2-8 U17 Socket Layout for 14-Pin and 8-Pin DIP Packages

Note: The clock generator must be 3.3 V type.

To select the on-board clock generator, JP8 should be jumpered from pin 1 to pin 8.The clock generator supplied with the DSP56305ADM is a 33 MHz oscillator in a 14-pin DIP package.

2.6.2 External Clock

To support non-standard clock rates and frequency fine tuning, an external clock input via a BNC connector is furnished. Using this connector, an external 3.3 V clock generator (50 ohm impedance, DC coupled), may be connected to the DSP56305ADM.

To avoid damage to the DSP, the external clock should be applied before the DSP56305ADM is powered on, and should be removed after the DSP56305ADM is powered off.

CAUTION

To avoid damage to the DSP56305 chip, ensure the DSP56305ADM is powered off when connecting or removing the external clock.

To select the external clock generator, JP8 should be jumpered from pin 3 to pin 6.

2.6.3 DSP56305 PLL Enable/Disable on Reset

The DSP56305 samples the PINIT / $\overline{\text{NMI}}$ line on exit from the reset state to determine whether the PLL should be enabled or disabled. To enable the PLL, JP2 should not be jumpered. To disable the PLL, install a jumper on JP2.The principles of $\overline{\text{NMI}}$ Request and PLL INIT selection are shown in **Figure 2-9**.

See **Table 2-8**.

Table 2-8 PLL Configuration Jumper Settings

Initial PLL Configuration	JP2
PLL Enabled	1 • • 2
PLL Disabled	1 $\boxed{\bullet\ \bullet}$ 2

During reset ($\overline{\text{RESET}}$ asserted), the level selected by JP2 is passed to the DSP by multiplexor U7. This level on $\overline{\text{NMI}}$ / PINIT is sampled by the DSP on the rising edge of $\overline{\text{RESET}}$, and latched into the PEN bit of the PLL control register. During normal operation ($\overline{\text{RESET}}$ deasserted), multiplexor U7 passes the $\overline{\text{NMI}}$ signal to the DSP. See **Figure 2-9**.

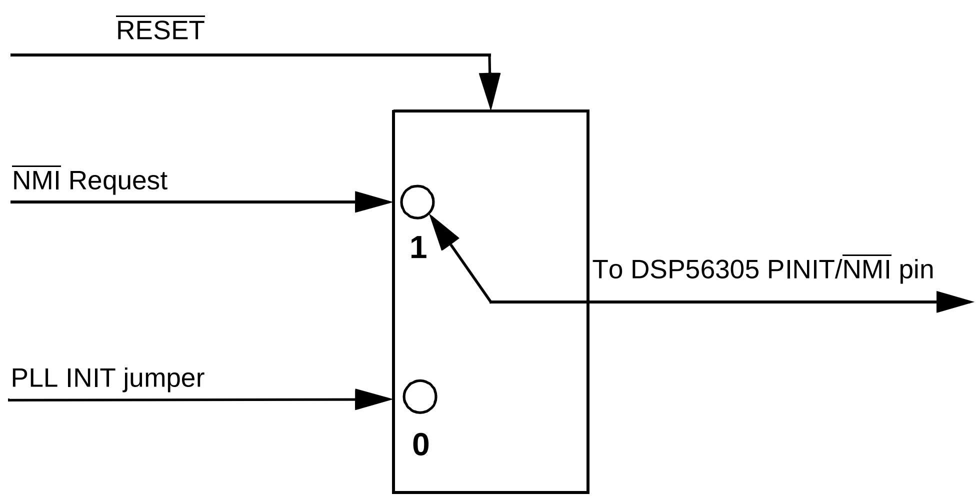


Figure 2-9 PLL Selection

After the $\overline{\text{RESET}}$ line is deasserted, the PINIT / $\overline{\text{NMI}}$ signal is connected to the $\overline{\text{NMI}}$ signal. The DSP56305ADM is factory configured for PLL enabled (JP2 removed).

2.7 HOST PORT SELECTION

The DSP56305's HI32 port supports the PCI bus with no n additional logic, while the ISA bus interface is supported with the addition of external buffers. To support application development on both platforms, DSP56305ADM supports both ISA and PCI environments. That is, the DSP56305ADM has edge connectors for both ISA and PCI, so the board can be plugged into any EISA / ISA or PCI host. The DSP56305ADM is factory configured for use with an ISA host.

When the DSP56305ADM is used in an ISA host, the default setting is used, and JP3, JP4, JP5, and JP6 are jumpered. U18, U20, U21, U22, U23, RN2, and RN3 are mounted in their sockets. See **Table 1-1** on page 1-6 for more information on jumper configuration.

When the DSP56305ADM is used as a stand-alone device, JP3, JP4, JP5, and JP6 should be jumpered; U18, U20, U21, U22, U23, RN2, and RN3 should be mounted in their sockets. The same configuration should be used for an ISA host.

When the DSP56305ADM is used in a PCI host, the jumpers on JP3, JP4, JP5, and JP6 should be removed. U18, U20, U21, U22, U23, RN2, and RN3 should be removed from their sockets.

2.7.1 ISA DMA and Interrupt Channel Configuration

The DSP56305ADM enables the user to configure one of four channels for DMA and one of four interrupt channels for the ISA bus interface. **Table 2-10** and **Table 2-12** describe these configuration options.

Table 2-9 ISA Bus DMA Channel Configuration

DMA Channel	J4	J5
0	8 • • • • 5 1 • • • • 4	8 [•] [•] • • 5 1 [•] [•] • • 4
5	8 • • • • 5 1 • • • • 4	8 • • [•] [•] 5 1 • • [•] [•] 4
6	8 • • [•] [•] 5 1 • • [•] [•] 4	8 • • • • 5 1 • • • • 4
7	8 [•] [•] • • 5 1 [•] [•] • • 4	8 • • • • 5 1 • • • • 4

Table 2-10 ISA Bus DMA Channel Configuration

DMA Channel	J4	J5
0	—	1–8, 2–7
5	—	3–6, 4–5
6	3–6, 4–5	—
7	1–8, 2–7	—

Table 2-11 ISA Bus Interrupt Selection

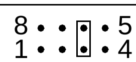
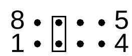
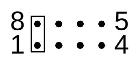
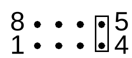
Interrupt	J6
5	
6	
7	
10	

Table 2-12 ISA Bus Interrupt Selection

Interrupt	J6
5	3–6
6	2–7
7	1–8
10	4–5

2.7.2 PCI Operation

The PCI bus is designed to operate with boards at a 3:5 frequency relationship. The standard PCI bus operates at 33 MHz, so the DSP56305ADM is configured to operate at 55 MHz.

The DSP56305 begins its boot routine after reset, which loads executable code from the Host to the board. When performed at 33 MHz, the boot routine located in the Bootstrap ROM is unable to change the Multiplication Factor (MF) in the PLL Control Register. The frequency relation of the PCI bus to the board is (3:3), and the DSP56305ADM cannot operate properly at this frequency ratio.

To allow operation using the PCI, configure SW3 for the Flash Boot mode. The code in **Example 2-1** must be programmed into the Flash memory. Following $\overline{\text{RESET}}$, the DSP56305 enters Flash Boot mode and loads this program from the Flash memory. The program changes theDSP56305ADM's initial frequency to the desired frequency, reconfigures the Operating Mode Register (OMR) for PCI configuration, and jumps to start of the boot routine. From this point, the DSP56305ADM performs its usual PCI operation.

Example 2-1 PCI Boot Flash Program

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;; bootpci.asm;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

; Boot from FLASH program setting Chip Frequency to 80MHz, turning chip
; to PCI mode by jumping to PCI boot segment in bootstrap ROM.
; To receive SREC format do next:
; >>> asm56300 -a -b -l bootpci.asm
; >>> srec -b bootpci

PLL_INIT_80          EQU     $750013          ; PLL Initialization Word - 80 MHz
M_PCTL
                     EQU     $FFFFFD     ; PLL Control Register
PCI_OP_MODE          EQU     $00000B      ; PCI mode configuration
BOOT_START          EQU     $ff0000        ; Starting address of bootstrap code

;******************************************************************************
; First two words in FLASH: Program size and Load_Run start address.
;******************************************************************************
            org     p:$0,p:$0
            dc      $120   ; The size of program
            dc      $000    ; Address in internal p: memory to load
                           ; program from flash and start to run.
```

Example 2-1 PCI Boot Flash Program

```
;***********************************************************************
;   Main Program
;***********************************************************************
            org     p:$0,p:
;***********************************************************************
;   Initialize PLL
;***********************************************************************

;****************************************************************************
movep   #PLL_INIT_80,x:M_PCTL   ; Activate PLL
        move                             omr,a
            and                                          #$FFFFF0,a
            or
#PCI_OP_MODE,a      ; set PCI mode
            move                  a,omr

        jmp                #BOOT_START   ; go to the bootstrap code beginning
```

2.8 CONNECTORS

The DSP56305ADM provides the following connectors:

- Expansion and logic analyzer connectors: 8×25 pin SMD pin-rows.
- Power: 3 pin terminal block, two-part
- HI32 port: ISA and PCI edge connectors
- SSI I/F: Two connectors, 2×7 and 2×15 SMD pin-rows
- JTAG/ OnCE port connector 2×7 SMD pin-rows

2.8.1 Expansion and Logic Analyzer Connectors

To support hardware expansion and logic analyzer connection to the DSP56305ADM, a set of four dual-in-line 50-pin SMD connectors is provided. All the DSP56305 pins are routed to these connector. In addition, contains +3.3 v and GND pins are provided to facilitate hardware expansions powered by the DSP56305ADM. These connectors are connected to most of the pins of the DSP56305 chip. The signals that are not provided on these connectors are: PCAP, XTAL, EXTAL, MODA, MODB,MODC, MODD and PINIT.

The pinout of these four connectors is shown in **Figure 2-10** on page 2-21 and **Figure 2-11** on page 2-22.

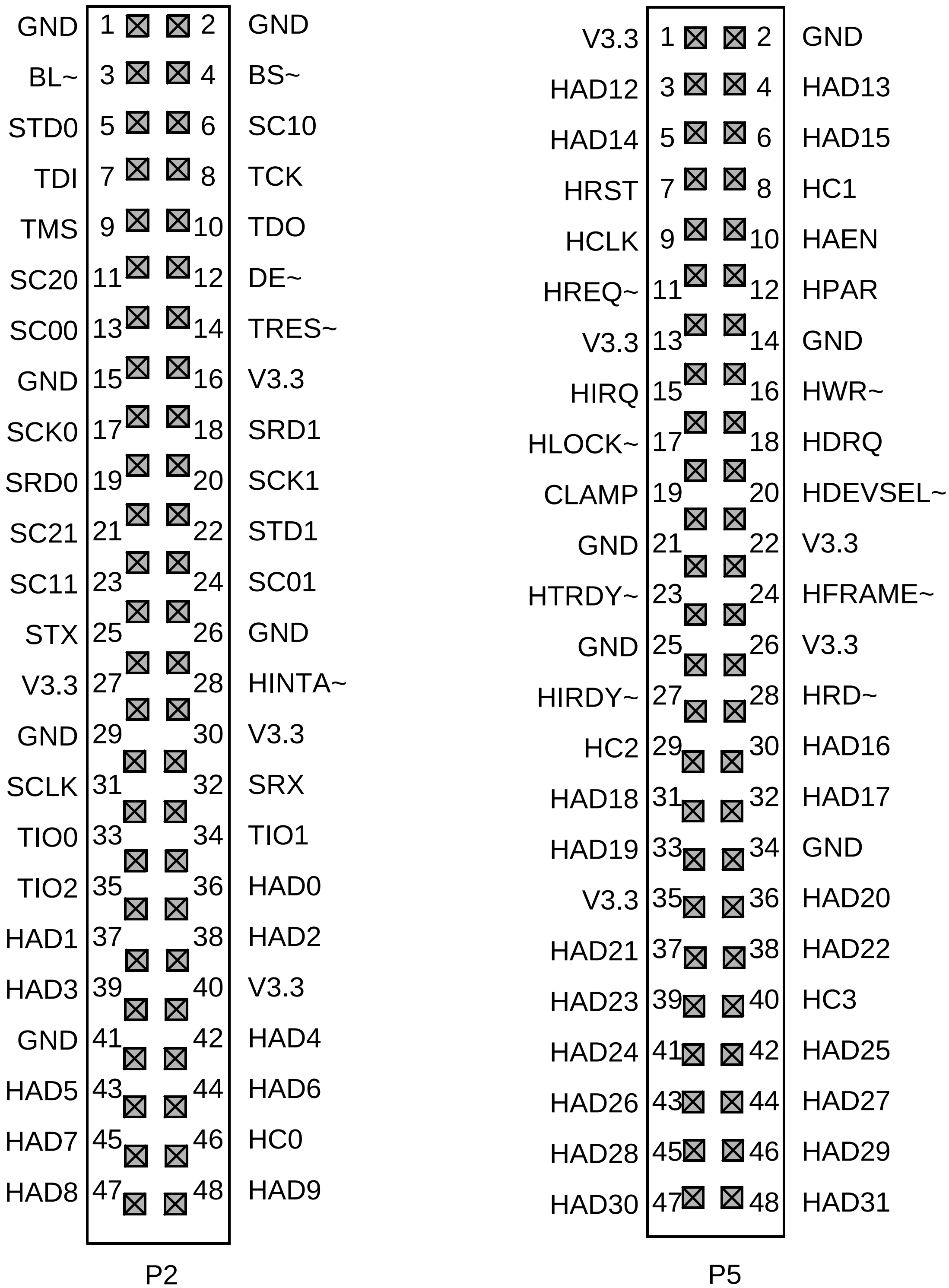


Figure 2-10 Expansion Connectors P2 and P5

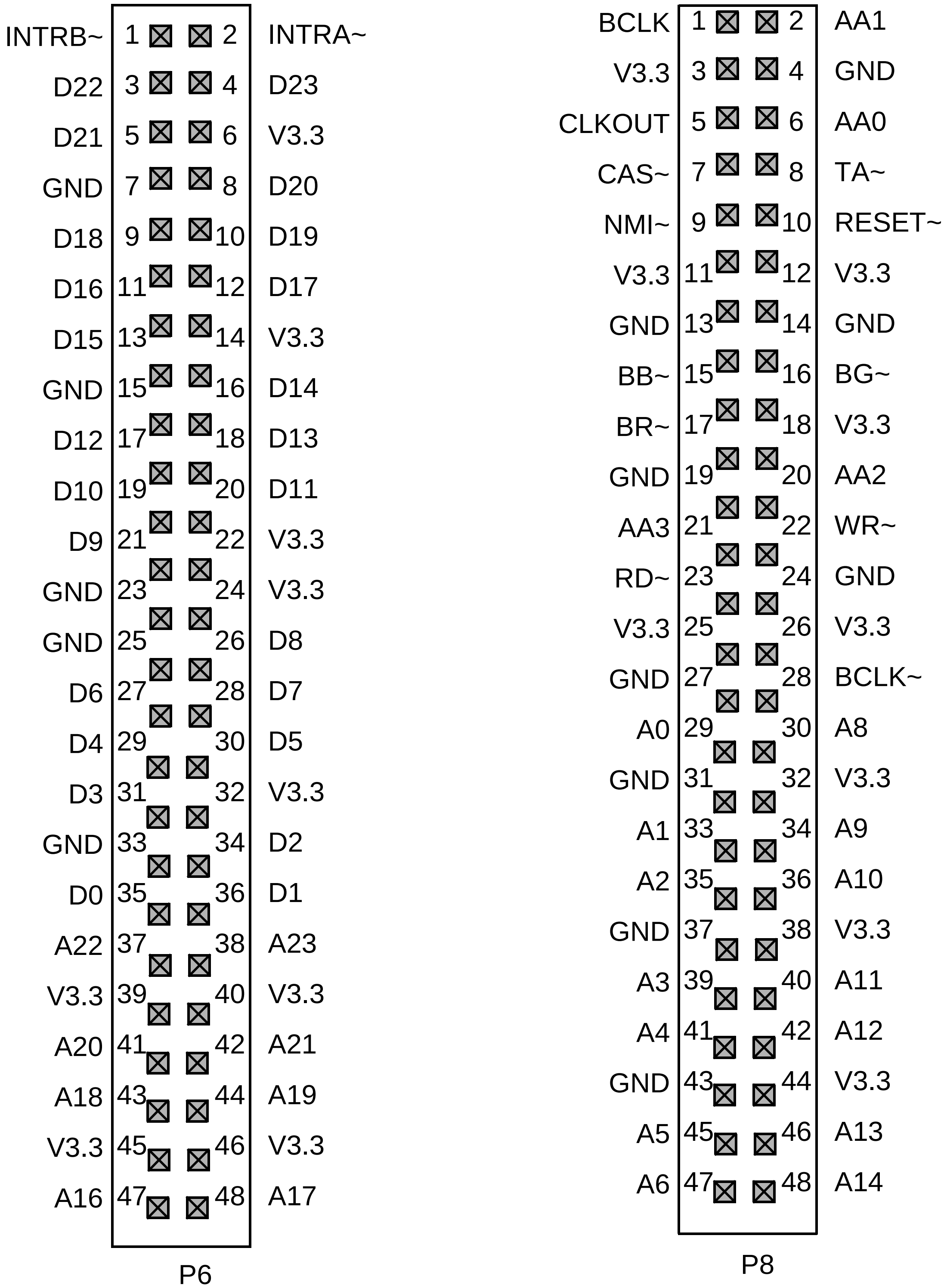


Figure 2-11 Expansion Connector P6 and P8

2.8.2 5 V Power Connector

The 5 V power connector to the DSP56305ADM is a 3-lead two-part terminal block connector. This two-part connector provides these advantages: It is easily detachable from the board, and connecting wires to it does not affect the soldering quality of its receptacle to the PCB.

The power connector is used only when the DSP56305ADM is used in stand-alone mode. If it is used in stand-alone mode, the power switch SW1 is used to turn the DSP56305ADM on and off. When installed in an ISA or PCI host, this switch is bypassed, and power is provided through the host interface connector.

2.8.3 HI32 Connector

Two HI32 connectors are provided on the DSP56305ADM, a PCI edge connector, configured as 32-bit universal (5 V and 3.3 V) connector, and an ISA edge connector. These connectors are located on opposite sides of the DSP56305ADM, enabling its operation in ISA, EISA, and PCI systems. The PCI edge connector is keyed with both 5 v and 3.3 v keys to allow operation in both 5 V and 3.3 V PCI systems.

2.8.4 SSI Port Connectors

The SSI port pins are provided on three different connectors:

- The Expansion and Logic Analyzer connectors
- Two dedicated SSI ports connectors
- DSP56004AIB compatible connector

The pins multiplication is to ease the connection of the SSI pins to various applications. The dedicated connectors are for general purpose use to be connected via a flat cable to another board. To avoid cross talk and to supply a constant impedance path for the ongoing signals, GND lines are inserted between the signal lines.

To avoid incorrect insertion of the receptacle connector, keying is provided as one of the pins is cut and its corresponding hole in the receptacle connector is filled.

The AIB interface connector supports the DSP56004AIB Audio Interface Board, which is a high-quality audio board with 2 stereo 18-bit ADCs and 3 stereo 18-bit DACs, originated for the DSP56004. The pinout of the independent SSI connectors and the AIB connector is shown in **Figure 2-13** on page 2-25 and in **Figure 2-12** on page 2-24. On the last figure, the most left column contains the AIB connector signals names, while the second to the left column, contains the DSP56305 signal names. When connected to the AIB card, the DSP56305ADM supports one stereo output channel and one stereo input channel.

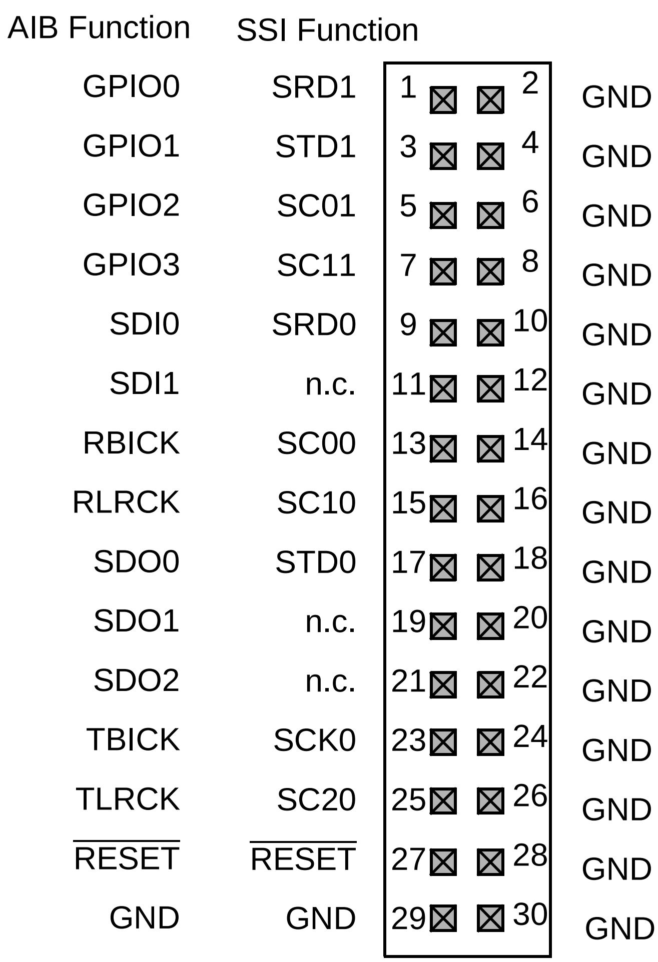


Figure 2-12 SSI—AIB Connector

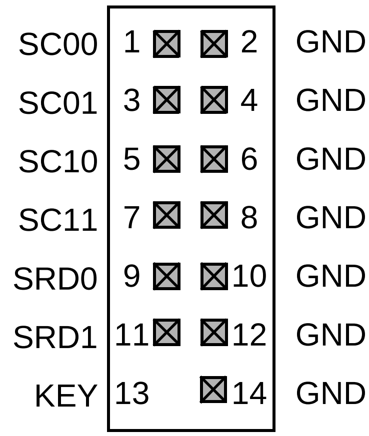


Figure 2-13 Dedicated SSI Connectors

2.8.5 SCI Port Connector

The SCI port pins are routed to two connectors:

- Expansion and logic analyzer connectors
- Dedicated SCI port connector

Routing to the expansion - Logic-Analyzer connectors is done to support expansion boards and application debug while the dedicated connector enables connection to an application board via a flat cable. To avoid incorrect insertion of the receptacle connector, keying is provided as one of the pins is cut while its corresponding hole in the receptacle connector is filled.

The pinout of the SCI dedicated connector is shown in **Figure 2-14** on page 2-25.

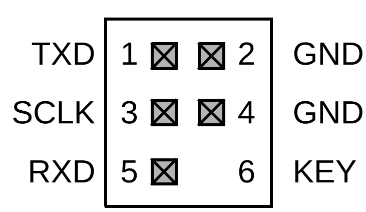


Figure 2-14 SCI Dedicated Connector

2.8.6 JTAG/OnCE Connector

The JTAG / OnCE connector is used both for JTAG testing during production, and for OnCE functions for code debugging and software development. The pinout of the JTAG / OnCE dedicated connector is shown in **Figure 2-15** on page 2-26.

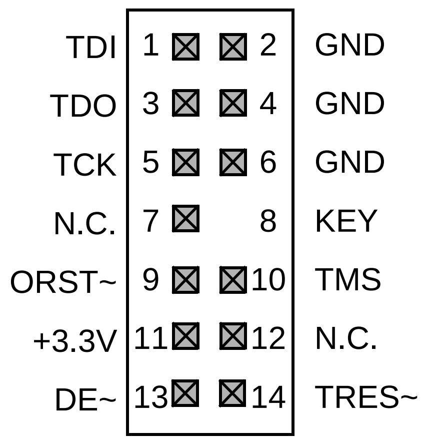


Figure 2-15 JTAG / OnCE Connector

APPENDIX A

DSP56305 SCHEMATICS

A.1 SCHEMATICS

Table A-1 provides a list of the schematics included in this appendix.

Table A-1 List of Schematics

Figure	Figure Name	Page
Figure A-1	SRAM Memory Bank #0	A-4
Figure A-2	Flash Memory	A-5
Figure A-3	Optional SRAM Bank #1	A-6
Figure A-4	DRAM Memory Bank	A-7
Figure A-5	ISA Bus Buffers	A-8
Figure A-6	PCI Connector	A-9
Figure A-7	JTAG, SCI, SSI, SSI–AIB Connectors	A-10
Figure A-8	Interrupts—Mode Control and Clock Supply	A-11
Figure A-9	CPU	A-12
Figure A-10	ISA Connector	A-13
Figure A-11	Decoupling Capacitors	A-14
Figure A-12	Expansions and Logic Analyzer Connectors	A-15
Figure A-13	5V–3.3V Power Regulator and Power up Reset Generator	A-16

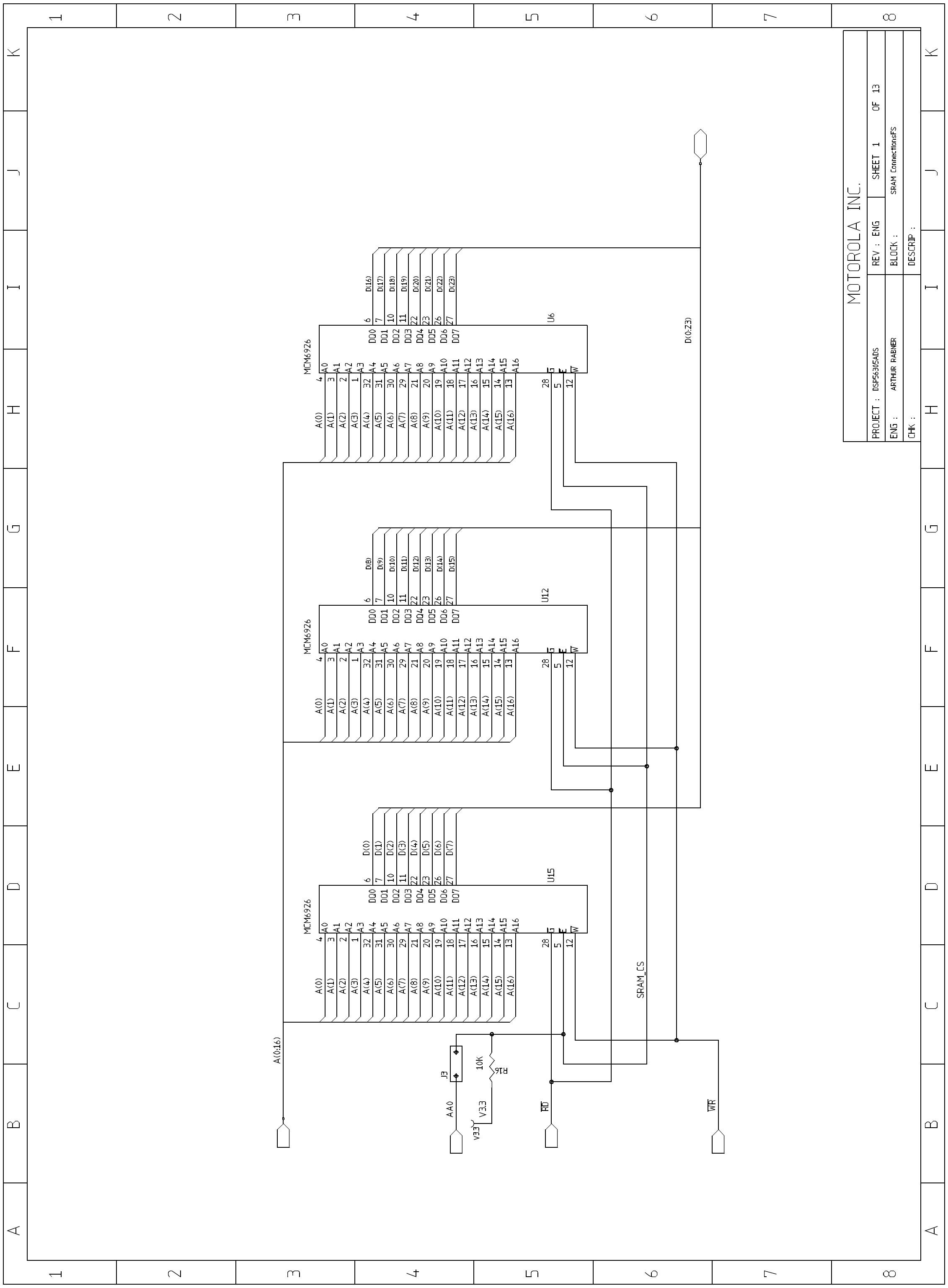


Figure A-1 SRAM Memory Bank #0

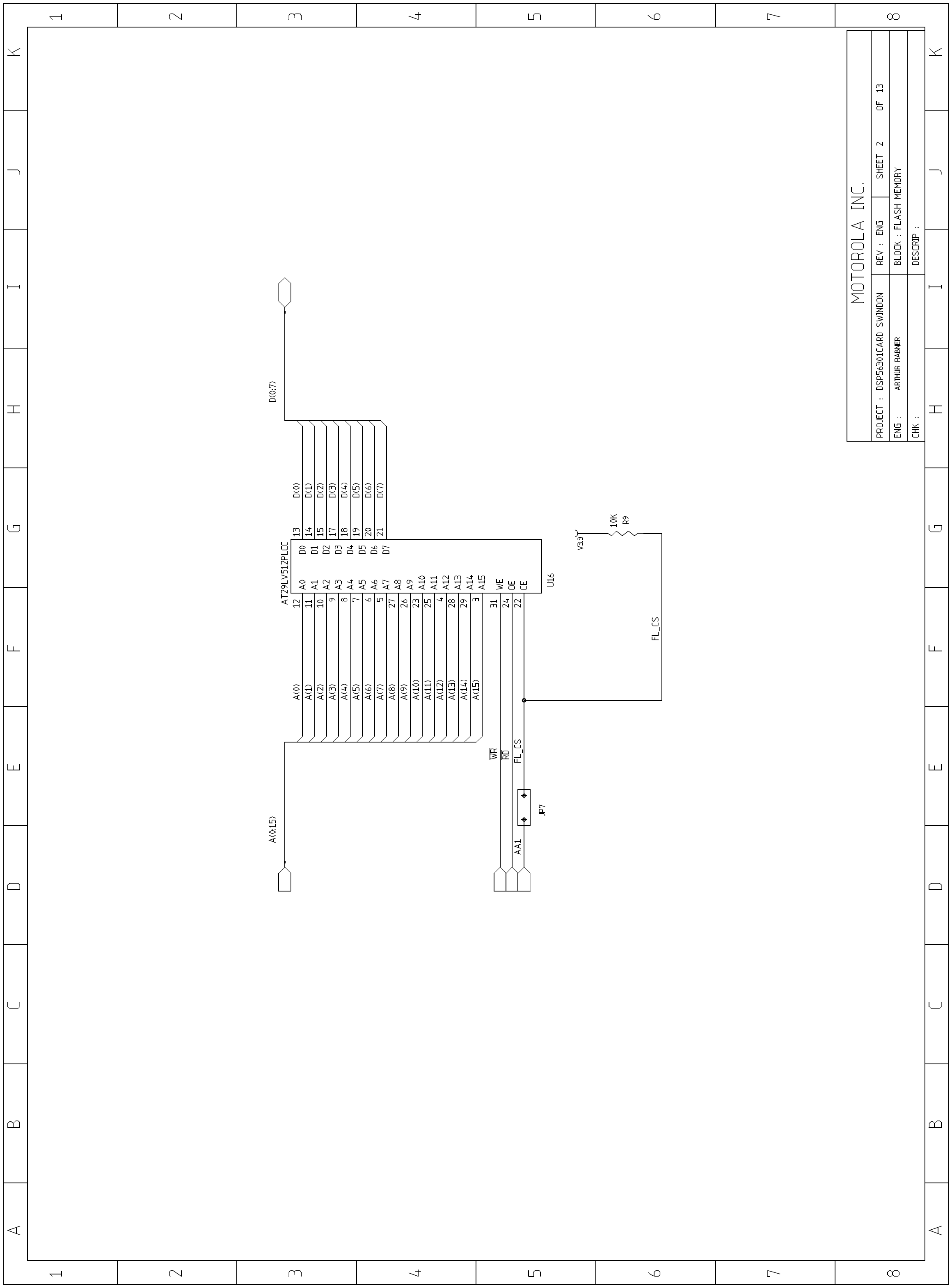


Figure A-2 Flash Memory

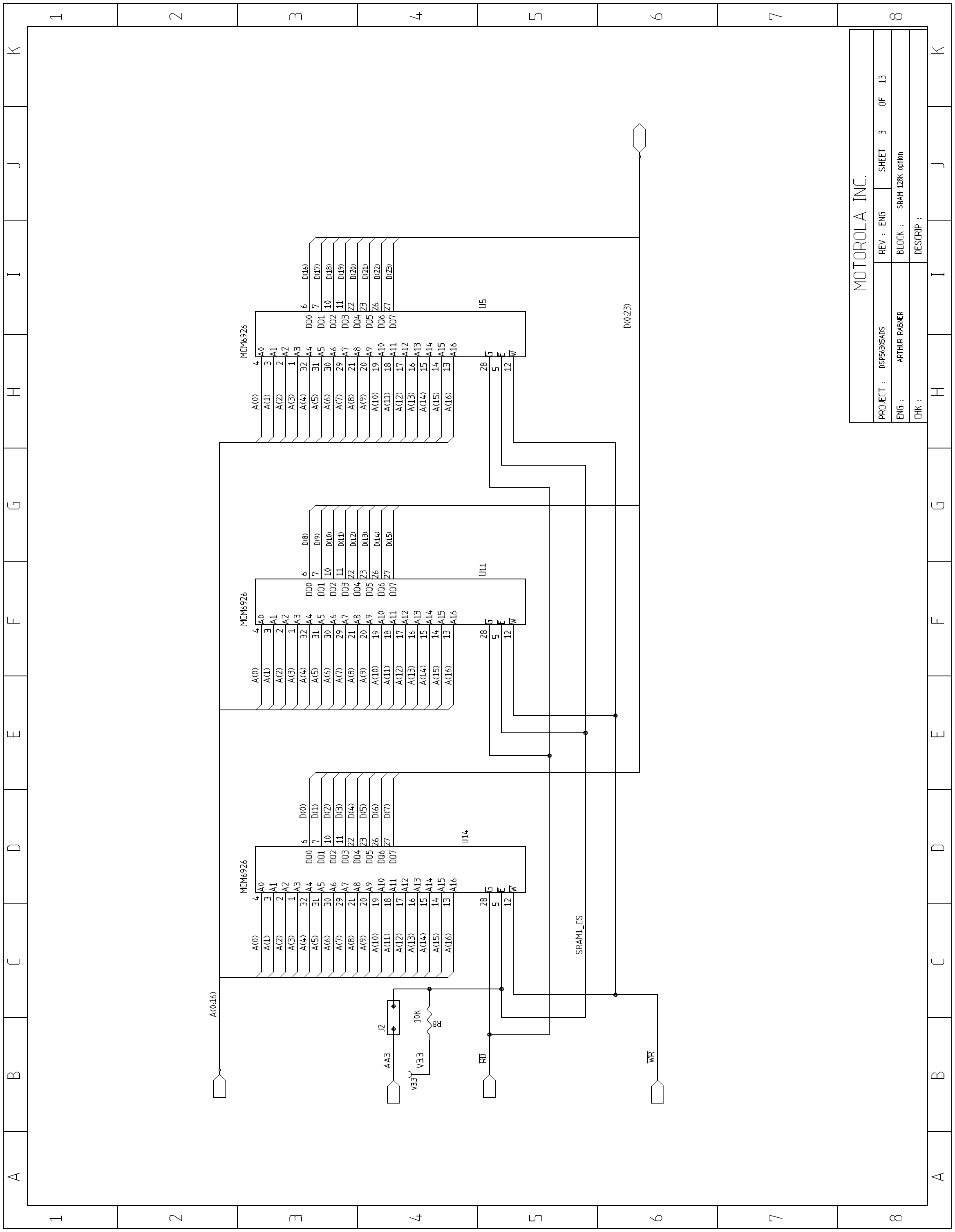


Figure A-3 Optional SRAM Bank #1

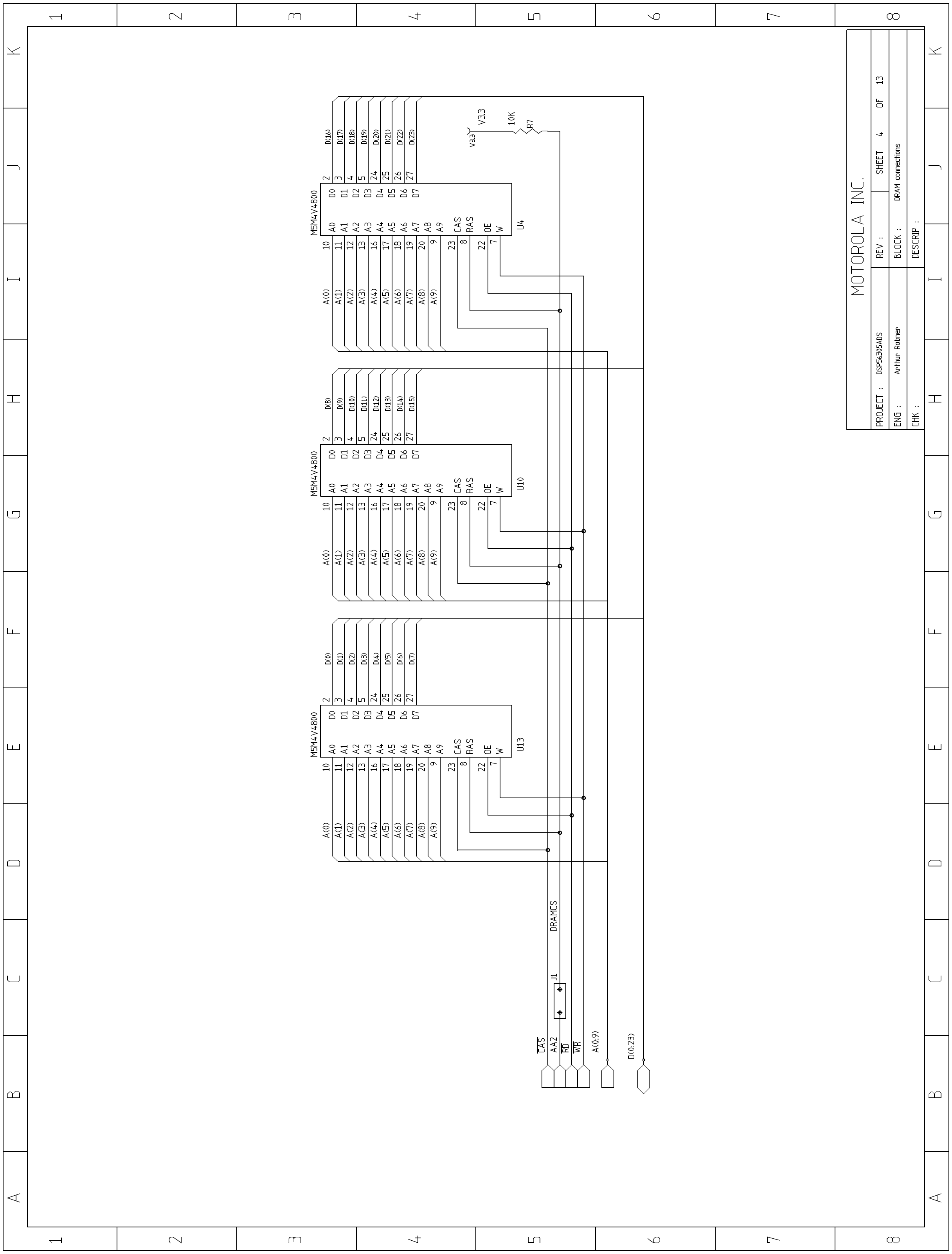


Figure A-4 DRAM Memory Bank

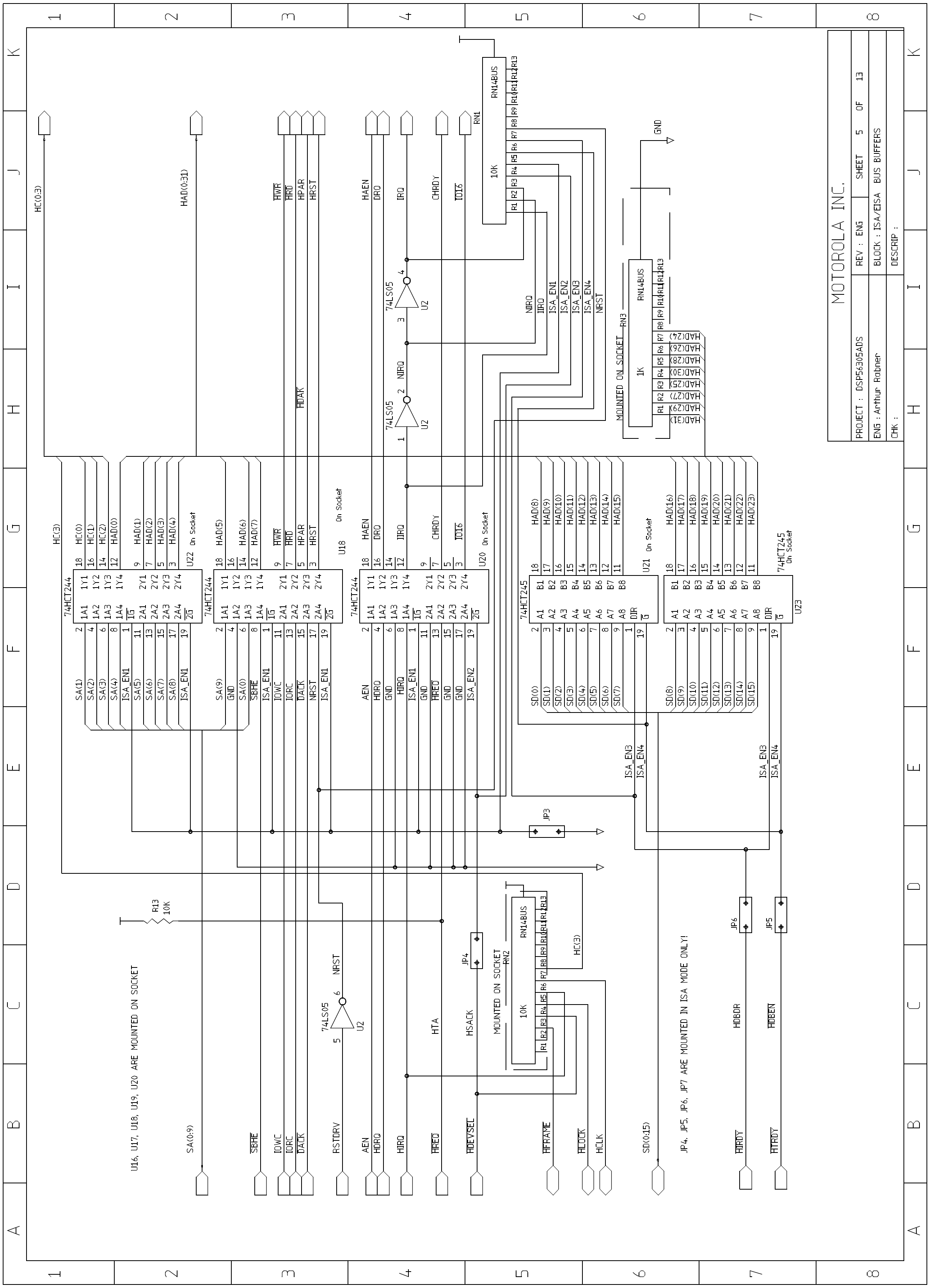


Figure A-5 ISA Bus Buffers

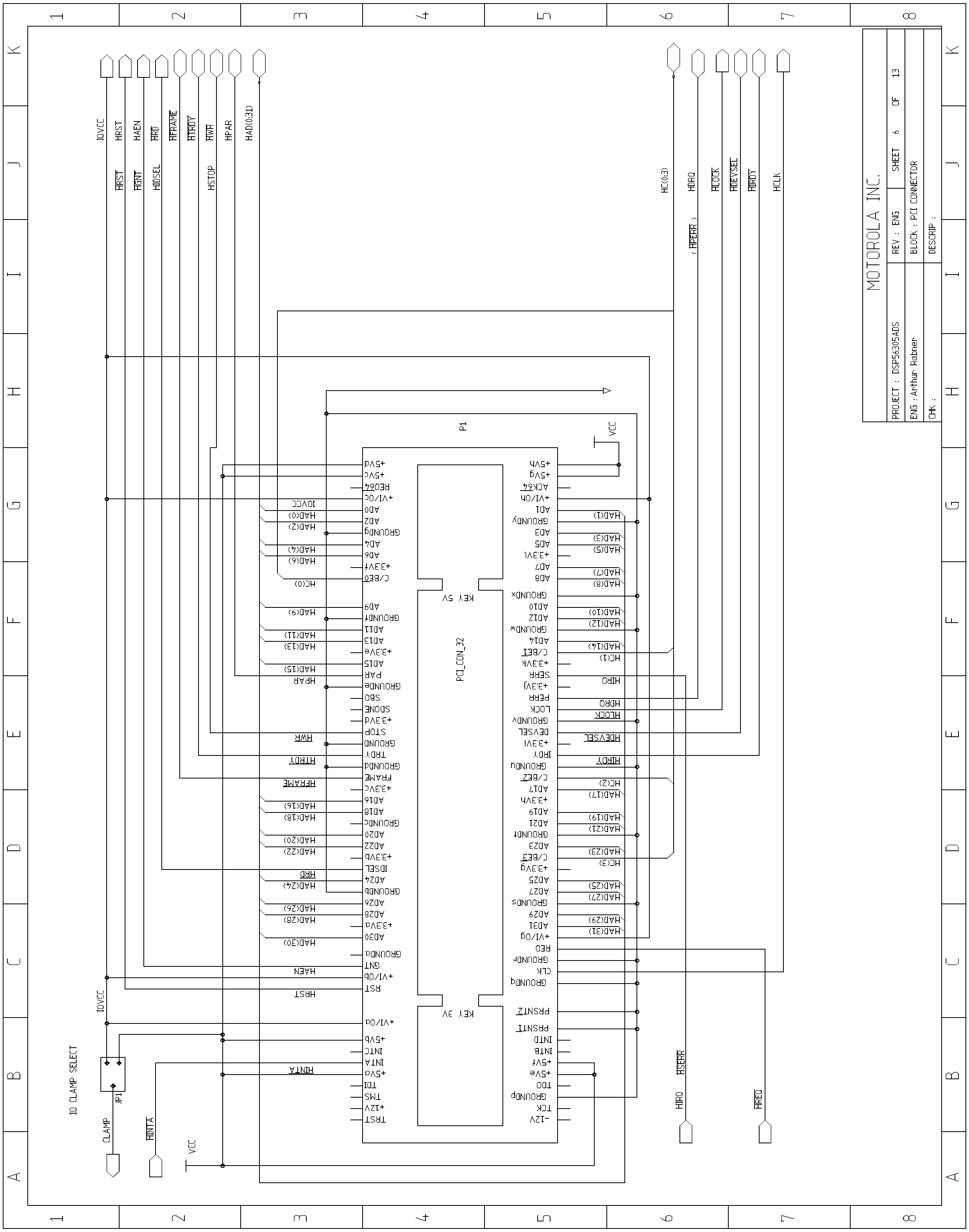


Figure A-6 PCI Connector

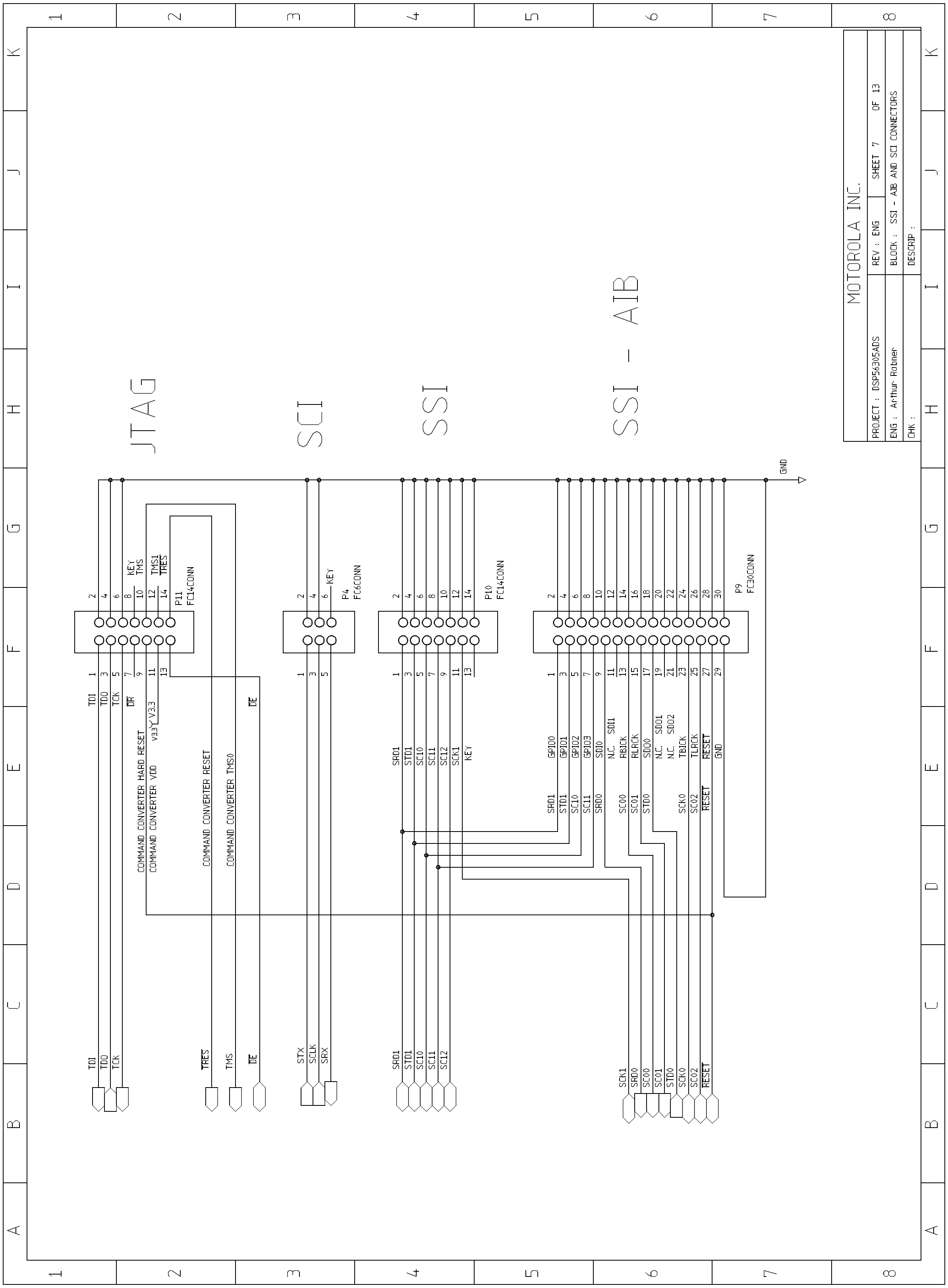


Figure A-7 JTAG, SCI, SSI, SSI–AIB Connectors

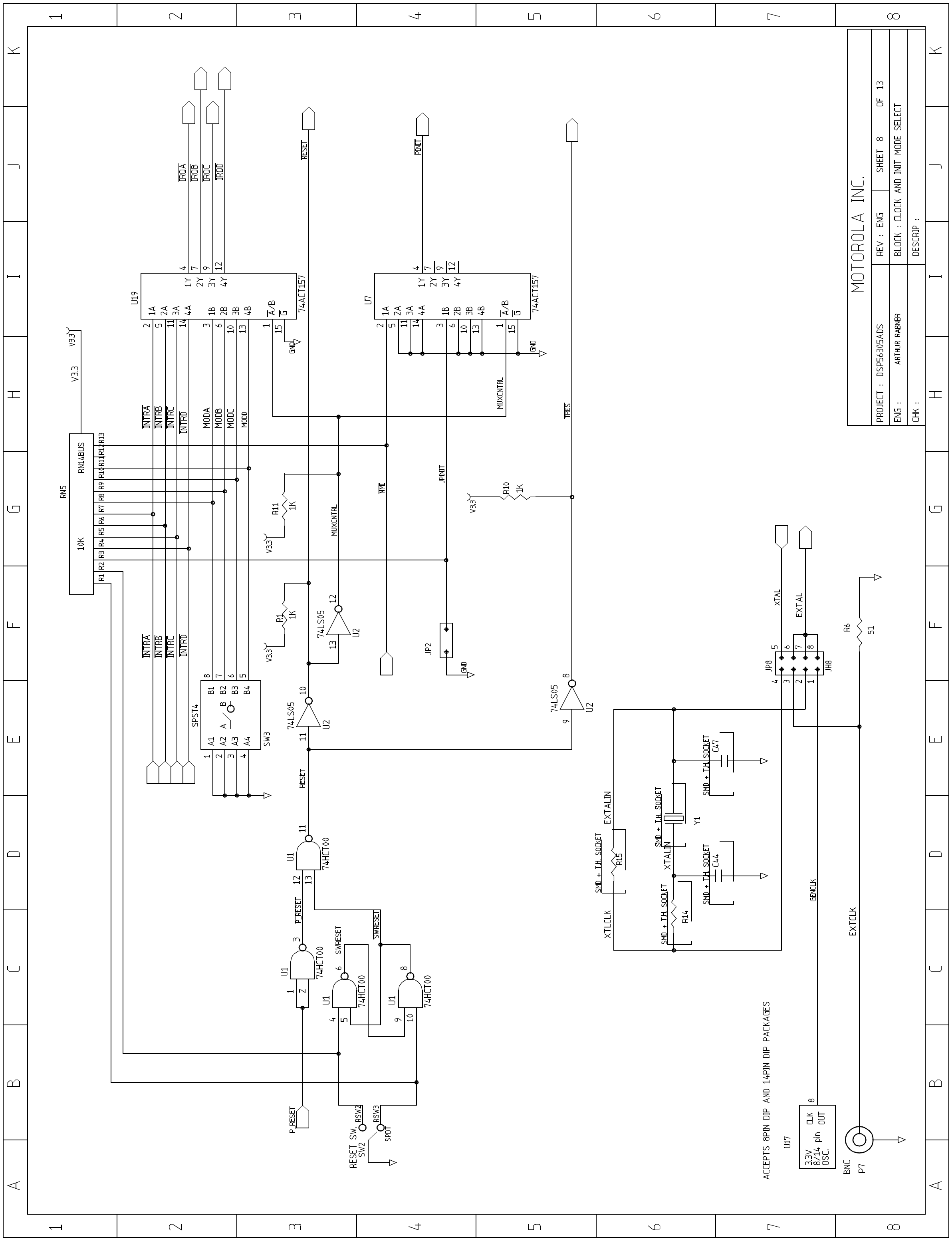


Figure A-8 Interrupts—Mode Control and Clock Supply

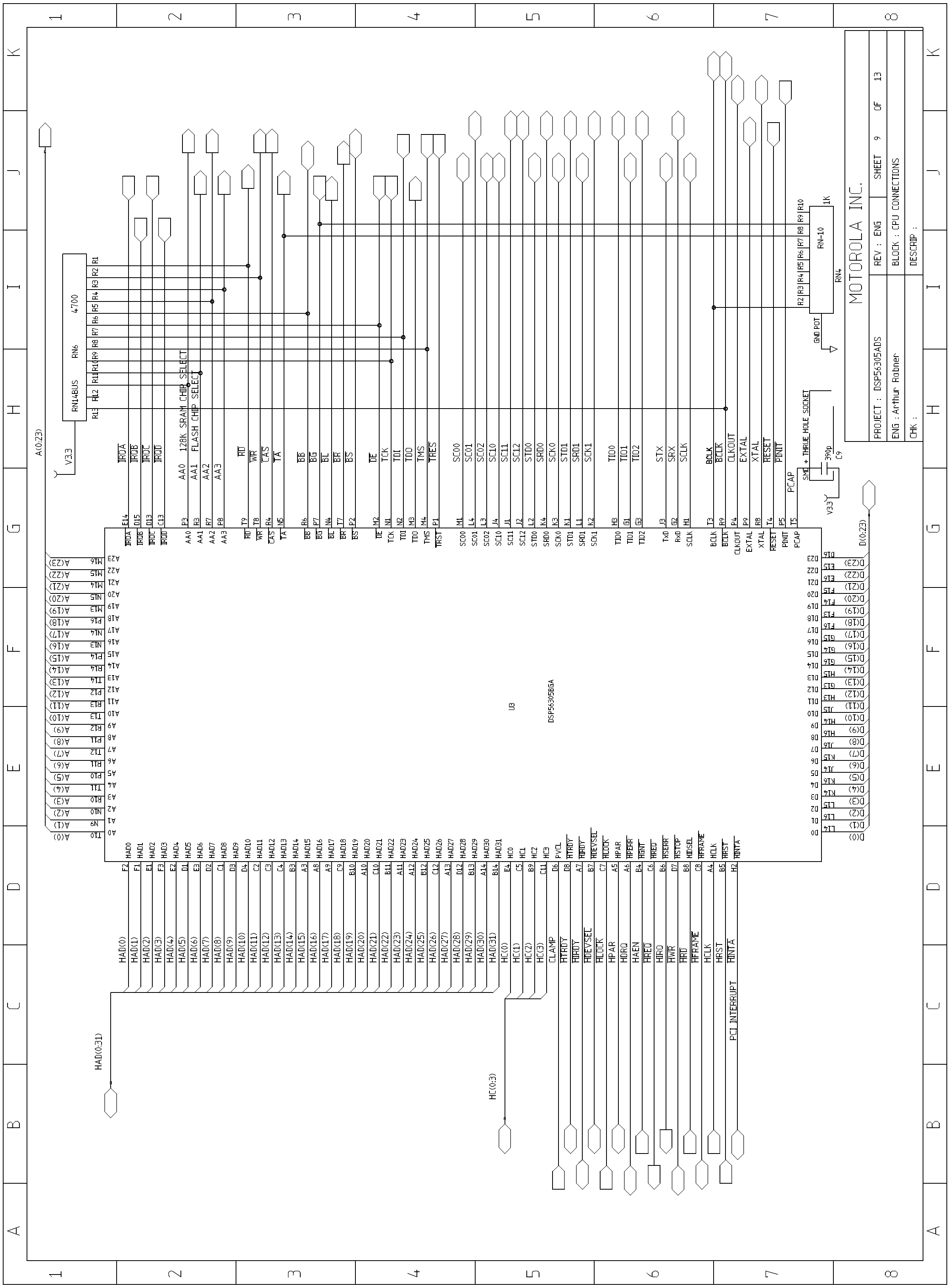


Figure A-9 CPU

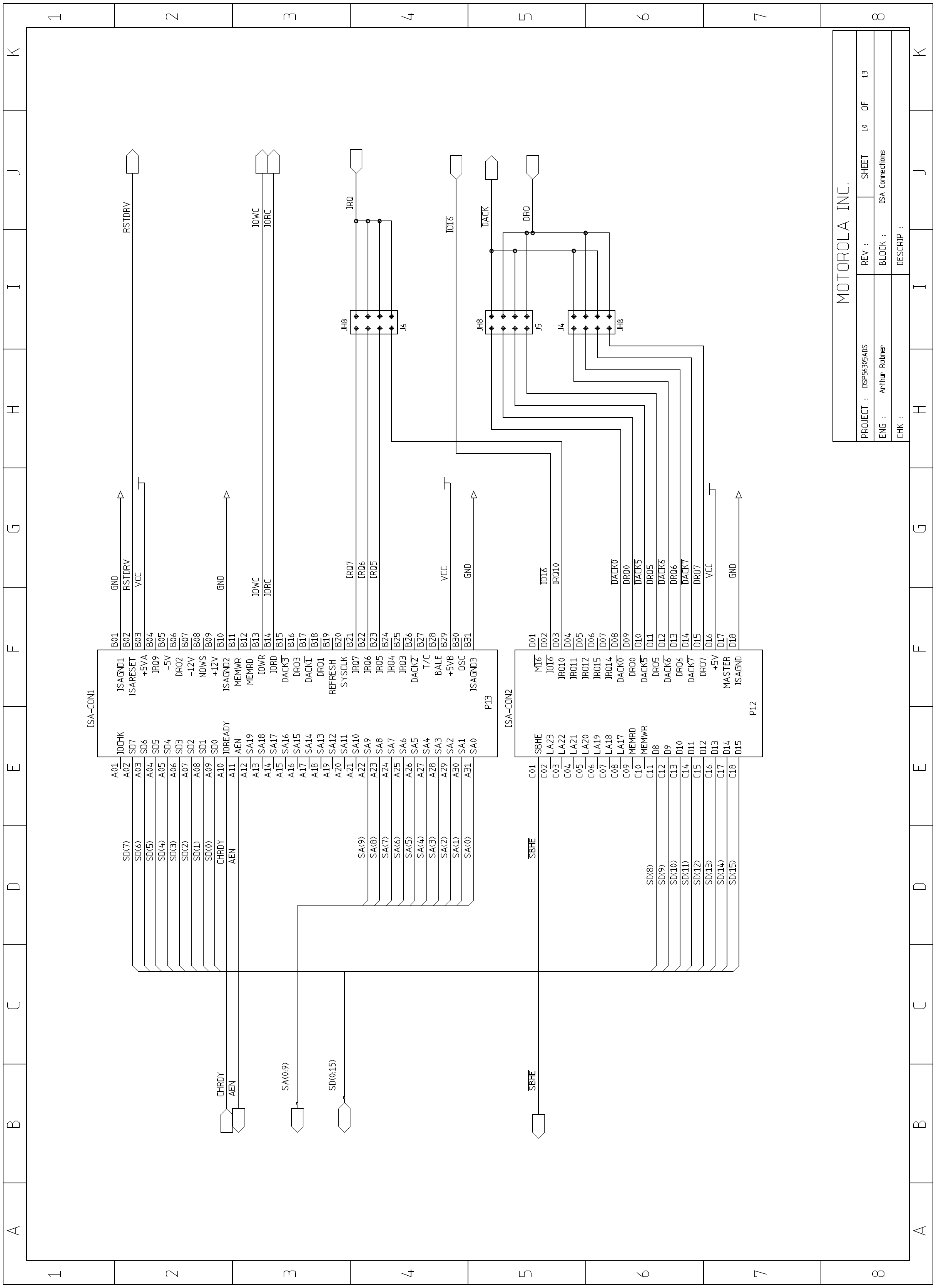


Figure A-10 ISA Connector

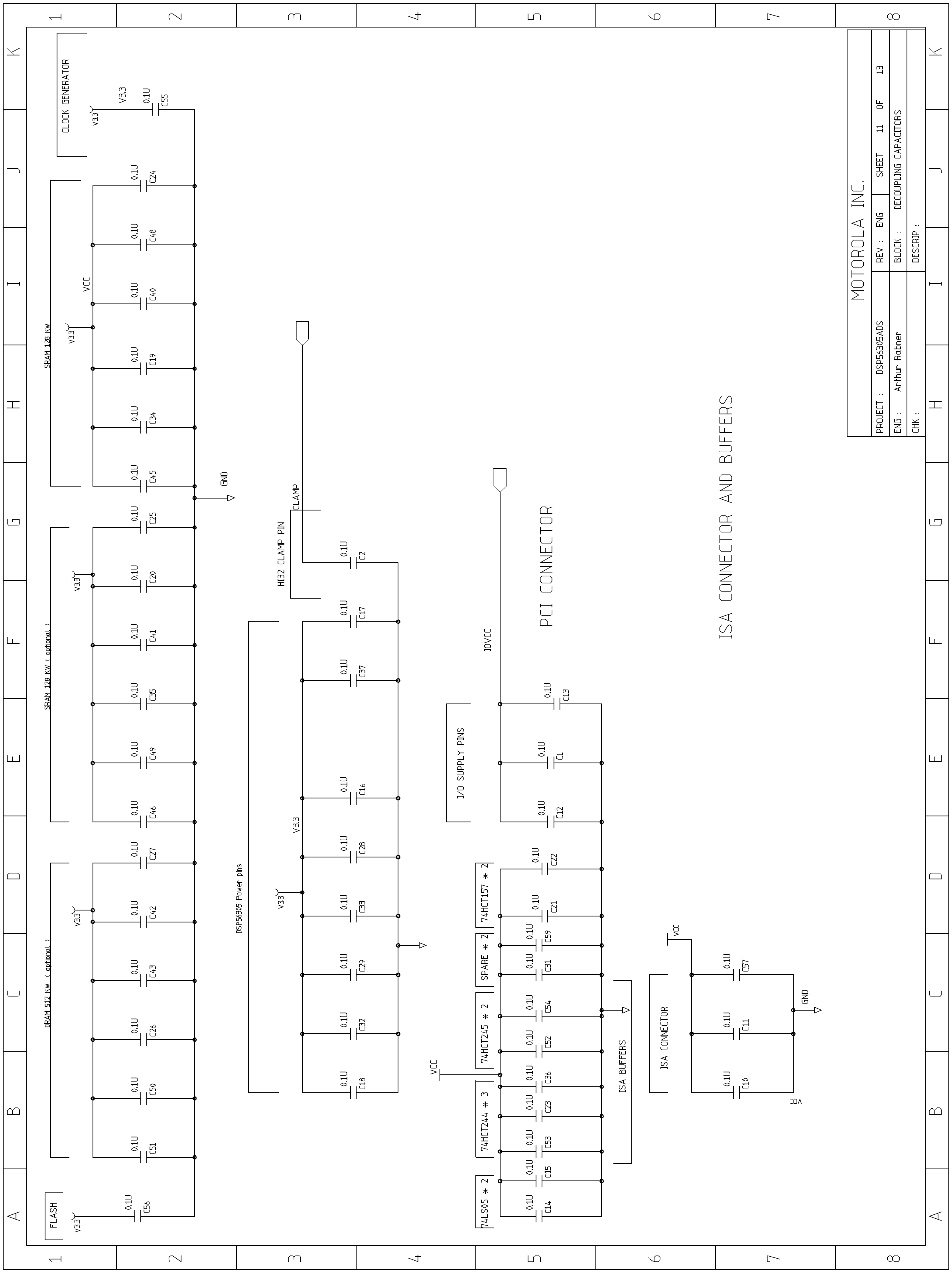


Figure A-11 Decoupling Capacitors

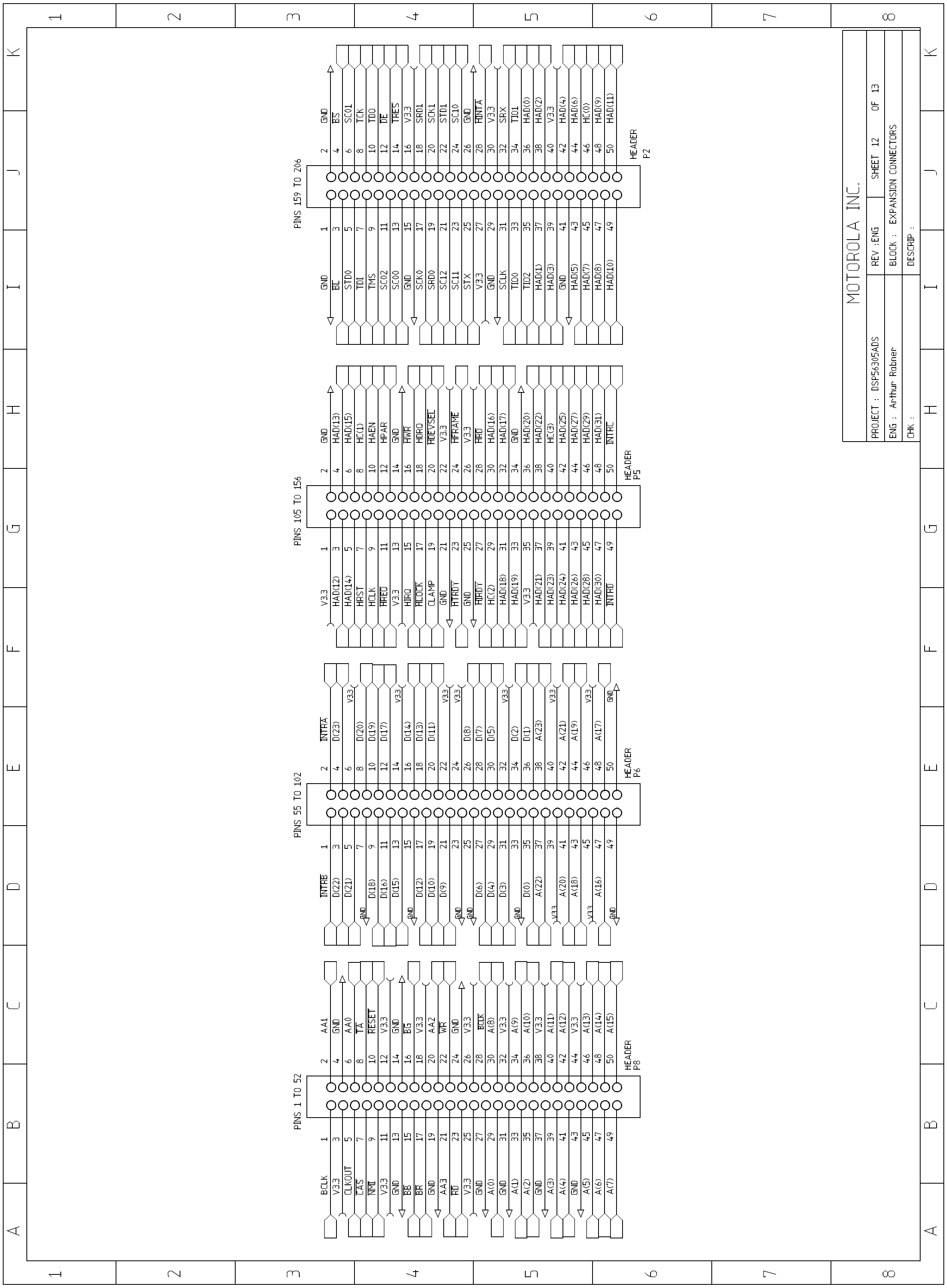


Figure A-12 Expansions and Logic Analyzer Connectors

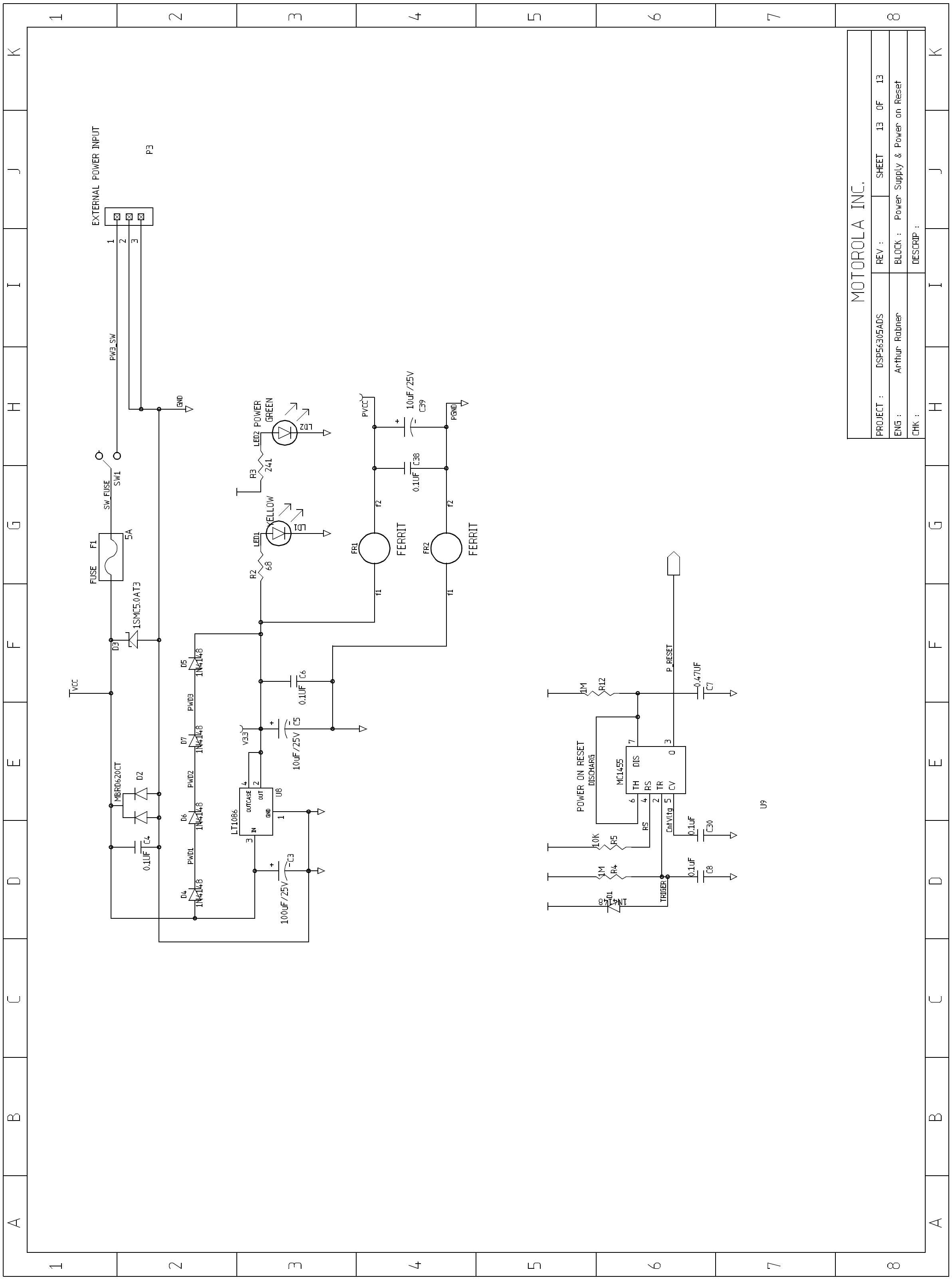


Figure A-13 5V–3.3V Power Regulator and Power up Reset Generator

APPENDIX B

DSP56305 BILL OF MATERIALS

B.1 BILL OF MATERIALS

Table B-1 Bill of Materials

Reference	Value	Description	MSIL Cat. No.	Total
C1, C2, C4, C6, C8, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C40, C41, C42, C43, C45, C46, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57	0.1 uF	VCAP	021-00064	51
C3	100 uF/10 v	DPCAP	023-00038	1
C5, C39	10 uF/20 v	DPCAP	023-00027	2
C7	0.47 uF	VCAP	021-00102	1
C9	390 pF	VCAP	021-00089	1
C44, C47	22 pF/20%	VCAP	021-00077	2
D1, D4, D5, D6, D7		1N4148	048-LL1N4148	5
D2		MBRD640CT	048-MBRD640CT	1
D3	1SMC5.0AT3	R1SDIO	048-1SMC5.0AT3	1
F1 on socket	5 A	Fuse	065-00025 015-00014	1
FR1, FR2		Ferrite	024-00013	2
J1, J2, J3, JP2, JP3, JP4, JP5, JP6, JP7		JMP2P	009-00165	9
J4, J5, J6		JH8	028-00148	3
JP8		JH8	009-00297	1
JP1		JMP3P	009-00165	1
LD1	yellow	LED	048-01003	1
LD2	green	LED	048-01001	1
P2, P5, P6, P8	Header (long pins)	FC50CONN	028-00136	4
P3		PWR3	009-00213	1
P4		FC6CONN	028-00147	1
P7		BNC	009-00287	1
P9		FC30CONN	028-00143	1

Table B-1 Bill of Materials (Continued)

Reference	Value	Description	MSIL Cat. No.	Total
P10		FC14CONN	028-00149	1
P11—remove pin 8		FC14CONN	028-00149	1
R1, R10, R11	1 KΩ	VRES	006-00257	3
R2	68 Ω	VRES	006-00288	1
R3	243Ω	VRES	006-00215	1
R4, R12	1MΩ	VRES	006-00249	2
R5, R7, R8, R9, R13, R16	10KΩ	VRES	006-00188	6
R6	51 Ω	VRES	006-00221	1
R15	3.9MΩ / 10%	VRES	006-00297	1
R14	200KΩ / 10%	VRES	006-00298	1
RN1	10KΩ	RN8 + VCC	051-00003	1
RN2 on socket	10K Ω	RN8 + VCC	051-00003 009-00027	1
RN5	10K Ω	RN14BUS	051-00046	1
RN3 on socket	1K Ω	RN8 + VCC	051-00014 009-00027	1
RN4	1K Ω	RN9 + VCC	051-	1
RN6	4700	RN14BUS	051-00036	1
SW1		Power On / Off	040-00032	1
SW2		Reset push button	040-00034	1
SW3		SPST4	040-00026	1
U1		74HCT00	051-74HCT00AD	1
U2		74LS05	051-74LS05D	1
U3 on 256-pin BGA socket		DSP56305BGA	051-	1
U4, U10, U13 *		M5M4V4800		3
U5, U11, U14		MCM6926		3
U6, U12, U15		MCM6926		3
U7, U19		74ACT157	051-74ACT157AD	2
U8		LT1086	051-LT1086CM	1
U9		MC1455	051-MC1455D	1
U16 on socket		AT29LV512PLCC	051- 009-00259	1

Table B-1 Bill of Materials (Continued)

Reference	Value	Description	MSIL Cat. No.	Total
U17 on socket	33 MHz	CLK_GEN_3V 8_14 pin	009-00262	1
U18, U20, U22 on socket		74HCT244	051-74HCT244 009-00290	3
U21, U23 on socket		74HCT245	051-74HCT245 009-00290	2
Y1	32.768 kHz	Crystal Oscillator	051-	1
Note: * Do not solder				